CHAPTER V
MEMORY SUBSYSTEM

SECTION 1
GENERAL DESCRIPTION OF THE MEMORY SUBSYSTEM

INTRODUCTION

The B 7700 Memory Subsystem provides the main storage for the B 7700 Data Processing System. The memory subsystem stores or supplies words of information as directed by either of two types of requestor: a central processor or an input/output processor.

A B 7700 Memory Subsystem is a modular configuration of one to eight memory modules coupled through a memory requestor switch/interlock network to a maximum of eight memory requestors. (See figure V-1-1.) The memory subsystem can service each requestor in the same manner so that any operation performed for one requestor may also be performed for any other requestor.

A memory module consists of a memory control module (MCM) cabinet which controls either one or two memory storage cabinets (MSC). The MCM controlling one MSC is identified as a 2-MSU memory module. The MCM controlling two MSC's is identified as a 4-MSU memory module. Each MSC contains: two independently addressable 2-1/2 D 2-wire core memory storage units (MSU). Each MSU consists of a memory storage module (MSM) with a storage capacity of 65,536 words (393,216 bytes); a memory logic module (MLM) for interfacing the TTL circuits of the MSU with the CTL circuits in the MCM; an independent memory power supply unit module for each MSU, and blowers for cooling.

Memory Capacity

A B 7700 Memory System may be built with various combinations of the two sizes of memory modules to achieve the desired total memory capacity. Table V-1-1 lists the possible combination of memory sizes.

MINIMUM MEMORY SIZE

The minimum memory size is one 2-MSU memory module of 131,072 words (786,432 bytes). This would be one MCM controlling one MSC containing two MSU's (65,536 words each). For optimum system performance the minimum B 7700 Memory Subsystem recommended is two 4-MSU memory modules. A failsoft system requires three memory modules.

MAXIMUM MEMORY SIZE

The maximum memory size is 1,048,576 words (6,291,456 bytes) which may be packaged as:

a. Eight 2-MSU modules

b. Four 4-MSU modules

c. A combination of 2-MSU and 4-MSU modules, the total of which equals 1,048,576 words.

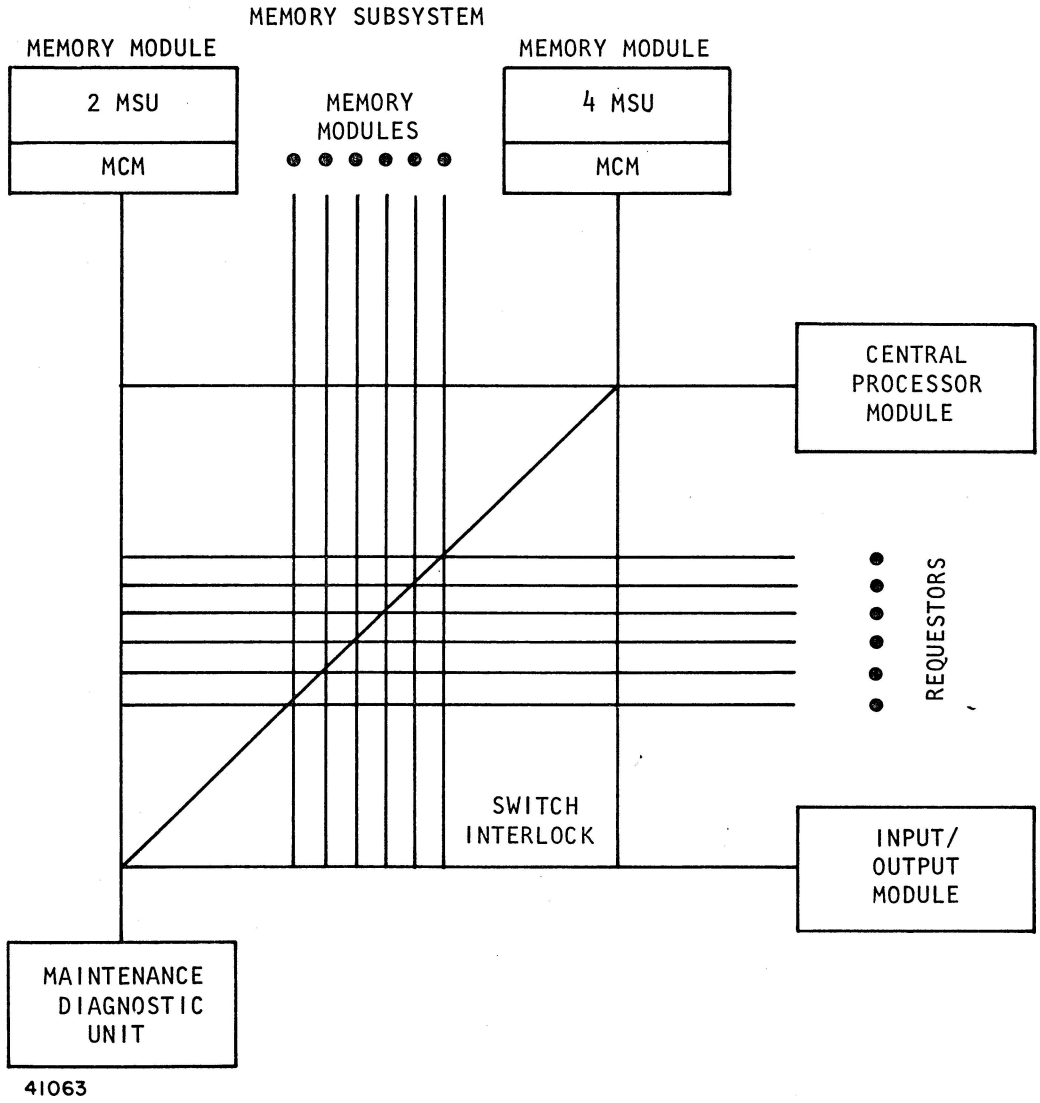


Figure V-1-1. B 7700 Memory Subsystem Modularity Diagram

Table V-1-1. B 7700 Memory Module Combinations

Memory Size		Memory Module Quantity		Memory Module Combination	
Words	Bytes	2-MSU Type	4-MSU Type	MCM	MSU
131,072	786,432	1	-	1	2
262,144	1,572,864	2	-	2	4
262,144	1,572,864	-	1	1	4
393,216	2,359,296	3	-	3	6
393,216	2,359,296	1	1	2	6
524,288	3,145,728	4	-	4	8
524,288	3,145,728	2	1	3	8
524,288	3,145,728	-	2	2	8
655,360	3,932,160	5	-	5	10
655,360	3,932,160	3	1	4	10
655,360	3,932,160	1	2	3	10
786,432	4,718,592	6	-	6	12
786,432	4,718,592	4	1	5	12
786,432	4,718,592	2	2	4	12
786,432	4,718,592	-	3	3	12
917,504	5,505,024	7	-	7	14
917,504	5,505,024	5	1	6	14
917,504	5,505,024	3	2	5	14
917,504	5,505,024	1	3	4	14
1,048,576	6,291,456	8	-	8	16
1,048,576	6,291,456	6	1	7	16
1,048,576	6,291,456	4	2	6	16
1,048,576	6,291,456	2	3	5	16
1,048,576	6,291,456	-	4	4	16

MEMORY CONFIGURATION

There are three memory module configurations recognized in a B 7700 Memory Subsystem: One MCM and four MSU's, one MCM and two MSU's, or, in case of a failure, one MCM and one MSU.

RECONFIGURATION

The B 7700 Memory Subsystem is designed with high reliability to minimize the occurrence of failure. Extensive error detection and reporting logic permits early capture of failures. Automatic correction of single-bit parity errors minimizes interruption to the system. The modular design, separate

power supplies, and redundant bussing concept permits soft reconfiguration. In case of an MSU failure the system can programmatically reconfigure the MSU's available to the MCM as follows:

a. The four-MSU memory module will be reconfigured to operate with only two MSU's available to the MCM as the cabinet containing the failed MSU becomes unavailable to the MCM.

b. The two-MSU memory module will be reconfigured to operate with only one MSU available to the MCM.

ADDRESS ALLOCATION

There is no specific assignment order within the system for particular MCM configurations. Memory module address range assignments are based on system requirements and are assigned through use of the memory limits word. For example, module 0 may be an MCM with two MSU's; module 1 may be an MCM with four MSU's, etc.

SUBSYSTEM ALLOCATION

The memory capacity may be programmatically allocated into subsystems by the operating system with respect to designated requestors, e.g., MCM's 0, 1, 2, 3, may be dedicated to requestors 0, 1, 2 while MCM's 4, 5, 6 may be dedicated to requestors 3, 4, and 5.

Clock Rate and Access Times

The B 7700 Memory Subsystem operates at a clock rate of 8 megaHertz. Access time for the MCM is 1.0 microsecond. The system read access time for the first word is 1.750 microseconds. (See tables V-1-2 and V-2-1.)

M.S.U. INTERLACING

Effective system read access time for two or more consecutive words is reduced by interlacing alternate MSU's in a memory module. This allows the second MSU to begin preparing for a memory cycle while the first MSU is completing transfer of its word. Thus, memory cycle overhead time due to the second, third, or fourth word is masked.

MULTIPLE-WORD TRANSFER (PHASING)

In a multiple-word transfer (known as phasing) words are transferred in bursts of up to four; one word is transferred at each clock cycle. Table V-1-3 shows the resulting decrease in effective memory system word read access time.

The maximum number of words which may be phased is set by the number of words that may be transmitted consecutively and is limited to the number of MSU's being controlled by the MCM; N=2 for the 2-MSU module and N=4 for the 4-MSU module. In each case, a limit is established by the MCM. If the requestor's word length exceeds the limit for a particular MCM, the MCM will:

a. Request only the number of words from the requestor allowable from its limit (in the case of storing information).

b. Send only the number of words to the requestor allowable from its limit (fetching data).

The limit in the MCM is established in the following manner:

a. Equal to single-word operation whenever the starting address from the requestor is within seven words from the end of the memory available to the MCM.

b. Whenever the starting address is greater than seven words from the end of the memory available to the MCM, the limit is equal to the number of MSU's available to the MCM.

The MCM limit does not have to be taken into consideration when generating a control word. For example, if a requestor desires a six-word operation, a control word with a word length field equal to six is generated.

The actual number of words transferred will be determined as described previously. The requestor must retain a record of the number of transfers remaining in order to determine if additional requests to the MCM are necessary to complete the operation.

Table V-1-2. B 7700 Memory System Read Access Time

Function	Time
Request to memory	0.1875 usec
Resolve priority, load control word	0.1250
Determine MSU's to initiate	0.1250
Information available from MU's	1.0000
Error check	0.1250
Data, MCM to requestor	0.1875
Total systems read access time (first word)	1.7500 usec

Table V-1-3. B 7700 Memory System Effective Read Access Times

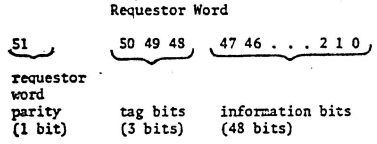
Access Function	Effective Read Access Time (usec) Total	Per Word	Per Byte
Single Word	1.750	1.750	0.291
Two Words	1.875	0.937	0.156
Four Words	2.125	0.531	0.088
Eight Words	4.250	0.531	0.088 (2-accesses)

Word Size

REQUESTOR WORDS

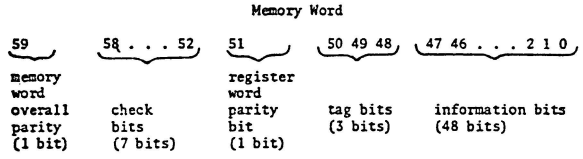
All words used by programs or system software in the B 7700 System are 48 bits in length. Three additional bits, called tag bits, identify the word as to whether it is used for code, data, or control. The tag bits allow hardware protection against incorrect usage of words and

are used by the hardware as a means for controlling many of the processing functions of the system. When information is passed from a requestor to an MCM, the requestor adds a parity bit which produces odd parity on the resultant 52-bit word being transferred. The MCM checks the word it receives for odd parity to verify that an error was not made during transmission.



MEMORY WORDS

A word as stored in an MSU consists of 60 bits. When an MCM receives a 52-bit word from a requestor, the MCM adds seven special parity bits, called check bits, and adds another bit for maintaining odd parity on the overall 60-bit word. The MCM then sends the 60-bit word to the MSU. (See figure V-1-2.) If a word should be accidentally altered while residing in an MSU, the seven check bits in conjunction with the overall parity bit allows for the detection of the error and provide a means for the automatic correction of errors in which a single bit has been altered.



Interface Signals

The signals used to transfer code, control words and data between the requestor and the MCM and between the MCM and the MSU are shown in figure V-1-3. Specific descriptions relative to the MCM-requestor interface are given in Section 2. The MCM-MSU interface is discussed in Sections 2 and 3.

Memory Addressing

Any requestor module can address up to 1,048,576 contiguous words of memory. These 1,048,576 words may or may not reside in consecutive memory modules.

Whether or not a particular requestor module is allowed access to a particular memory module depends on the setting of a bit in the requestor inhibit register. The requestor inhibit register contains 8 bits, one bit for each of the 8 possible requestors. Thus, a particular memory module can be shared by all requestors, some requestors, or can be the exclusive resource of only one requestor.

By setting the requestor inhibit registers of particular groups of memory modules to allow access by only selected requestors, it is possible to logically divide the system into several separate processing subsystems, each perhaps with its own MCP and each perhaps dedicated to a specific part of the total processing load. The hardware unit numbers for the requestor modules are zero through seven. The bit position of the requestor inhibit register corresponds to the requestor unit number, with zero as the least significant bit. If a requestor inhibit bit is ON in the requestor in-

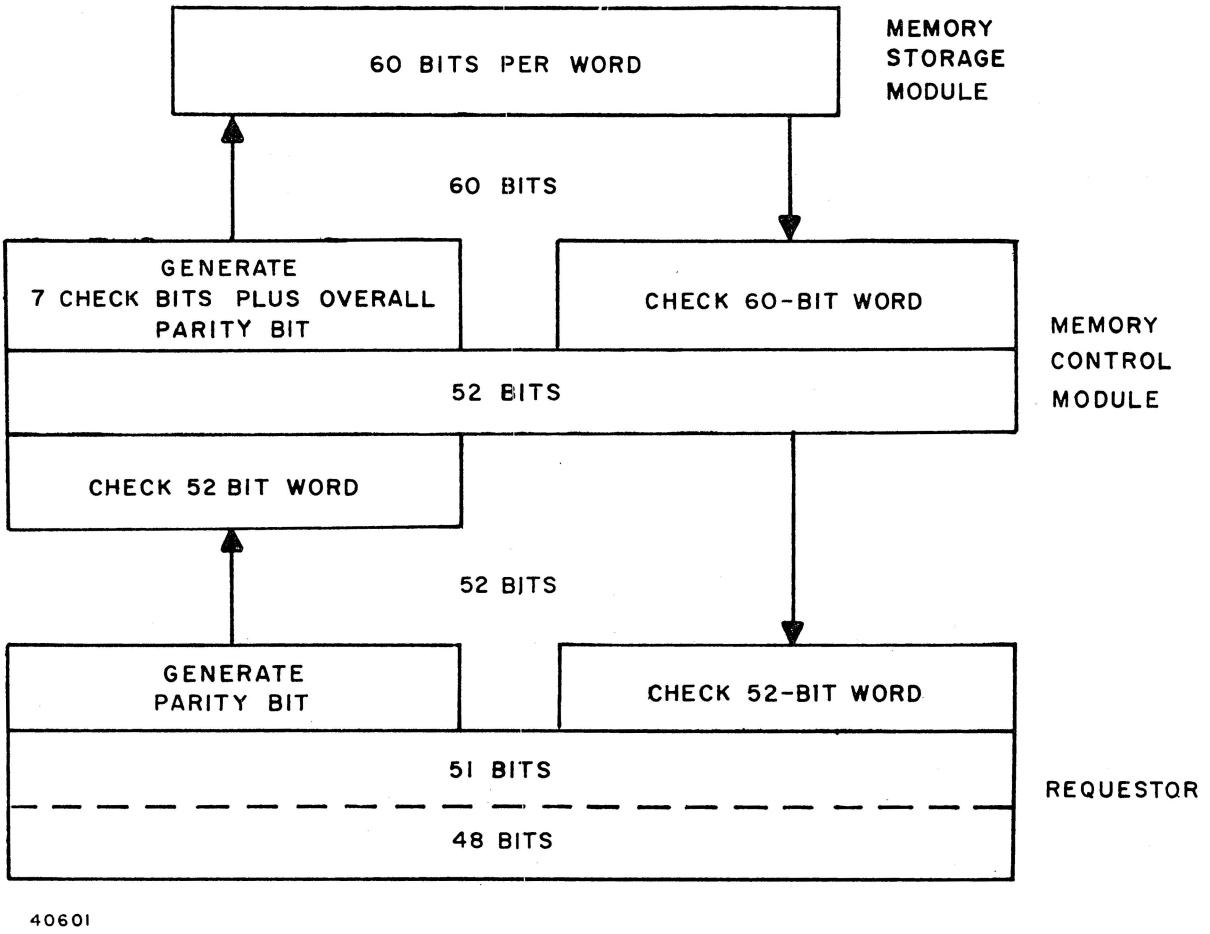
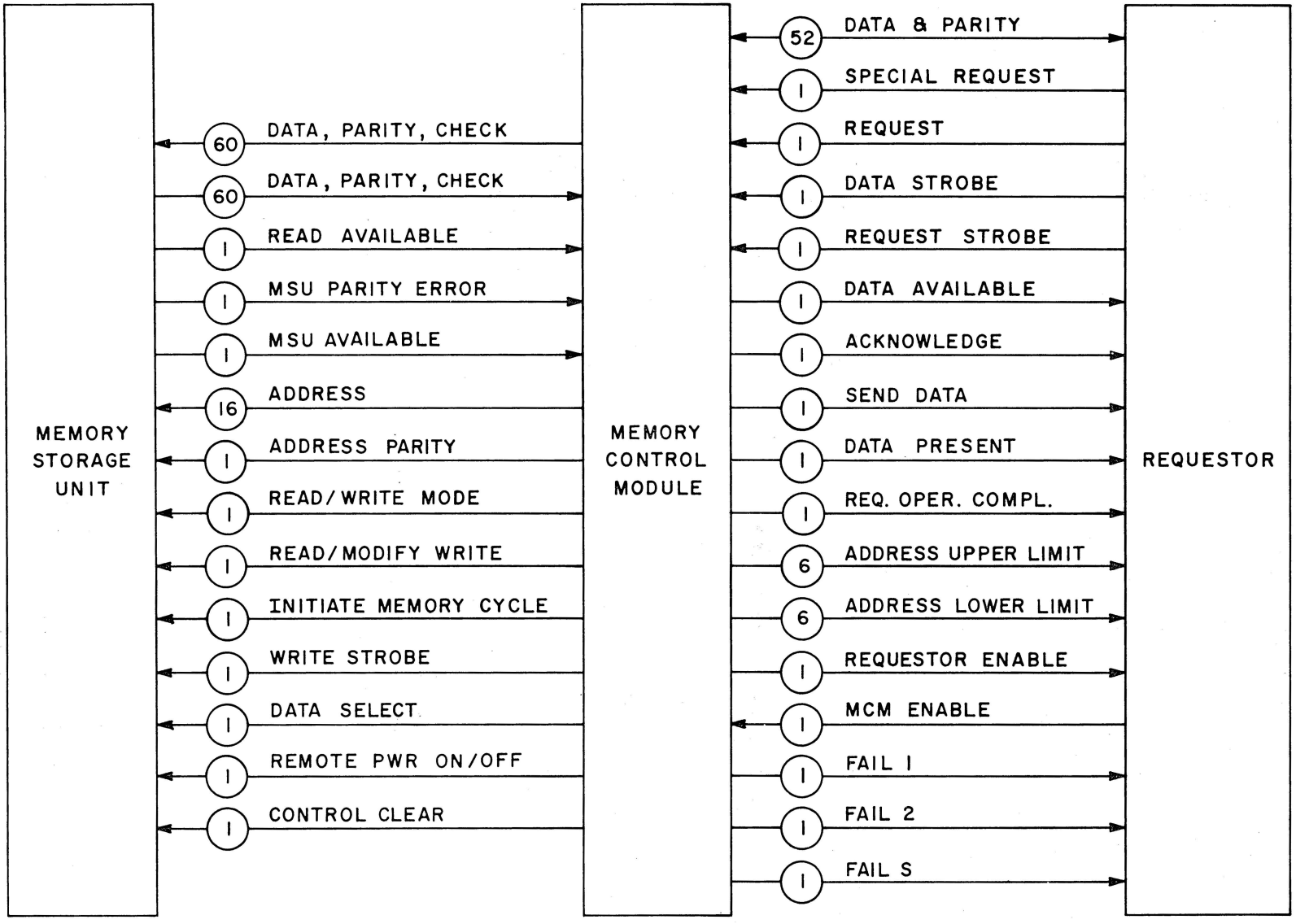


Figure V-1-2. Data Word Transfer Between Requestor and Memory



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Figure V-1-3. Requestor-MCU-MSU Interface

hibit register, the unit corresponding to the bit is denied access to the memory module. The requestor inhibit register is set by the load requestor inhibit register instruction. This instruction may be executed only by the MCP. The MCP is therefore able to alter the configuration of the system according to changing requirements.

The amount of usable memory within a memory module may vary from 65,536 words, with only one MSU operational, to 262,144 words with four MSU's operational. Addressing within a memory module is controlled by two memory limit registers which specify the lowest and highest addresses available. The highest address available is always 16,383 addresses higher than the address indicated in the upper limit register.

Each memory limit register is 6 bits in length. The memory control module "sees" the memory contained in a memory storage unit as a number of 16,384-word segments.

A memory address consists of 20 bits, the first 6 of which designate a 16,384-word memory segment within the 1,048,576 words which any one requestor can address. The other 14 bits are used to address the word within the designated segment. The most significant 6 bits of a memory address are compared against the 6 bits of each of the two memory limit registers to determine whether the specified address exists within the MSU's assigned to the MCM.

The memory limits registers are set by the load memory limits instruction. This instruction may be executed only by the MCP. The MCP determines the amount of memory assigned to an MCM during system initialization by accessing memory within successively higher 16,384-word segments. The MCP then sets the memory limit registers accordingly. If an MSU or an MCM fails, the MCP is informed of the failure. The MCP can change the memory limit registers to avoid using a faulty MSU, or can set the requestor inhibit register to avoid accessing the memory module altogether.

By setting requestor inhibit registers and memory limit registers, groups of memory modules can be masked to form separate memory systems, some perhaps with the same span of addresses. In this way, critical data or program code can be duplicated to provide additional protection against system failures.

SECTION 2
MEMORY CONTROL MODULE

GENERAL DESCRIPTION OF MCM

The MCM links all requestors (input/output modules (IOM's) and Central Processor Modules (CPM's)) with the MSU's which the MCM controls. The maximum number of MCM's per system is eight.

MCM Logic Functions

The logic functions of the MCM are: priority resolution, data transfer and control, and error detection. (See the block diagram in figure V-2-1.)

PRIORITY-RESOLUTION LOGIC

Priority-resolution logic controls communications between each requestor and the MCM. Only those requestors selected by the state of the requestor-inhibit register are allowed to be serviced by the MCM. The exception to this rule is that through the use of the special-request signal, CPM's are able to override the state of the requestor-inhibit register. The order of servicing these requestors (priority) is determined for maximum efficiency of a B 7700 System. Lower user priorities (i.e., higher numbers) are assigned to central processor modules. For example, in a system with two CPM's and two IOM's, the CPM's would be assigned priorities 6 and 7 and the IOM's would be assigned priorities 0 and 1. A requestor is eliminated from servicing if the requestor's interface has failed so that other requestors are locked out. The highest-priority requestor is prevented from obtaining consecutive services if a lower-priority requestor is waiting to be serviced.

DATA-TRANSFER-AND-CONTROL LOGIC

The data-transfer-and-control logic provides the sequential control signals required to route the data between the requestor and the MSU. This logic provides the capability of time-phasing words between the requestor and memory at the clock rate.

ERROR-DETECTION LOGIC

The error-detection logic detects errors in requestor and MSU inputs; records errors in the fail register and notifies the requestor that the error occurred; and corrects one-bit errors that occur in the MSU during a fetch operation.

MCM Communications

All communications between the MCM and the requestors are applied thru 78 separate bidirectional lines to identical switching interlock receiver/driver circuits located in each requestor module. (See Figure V-1-3.) A set of 52 lines is used for both the control words and the data words. During operation, the control word always precedes the data word, and consequently both words are never on the line at the same time.

When a requestor desires access to an MCM, a request signal is sent to the MCM. The priority resolver circuits determine if the MCM is busy with another requestor or if that requestor is inhibited from accessing this particular MCM. If access is permitted, a request strobe in coincidence with a control word is sent to the MCM to initiate the timing and to instruct the MCM that either a read, write or a read memory write operation is to be performed.

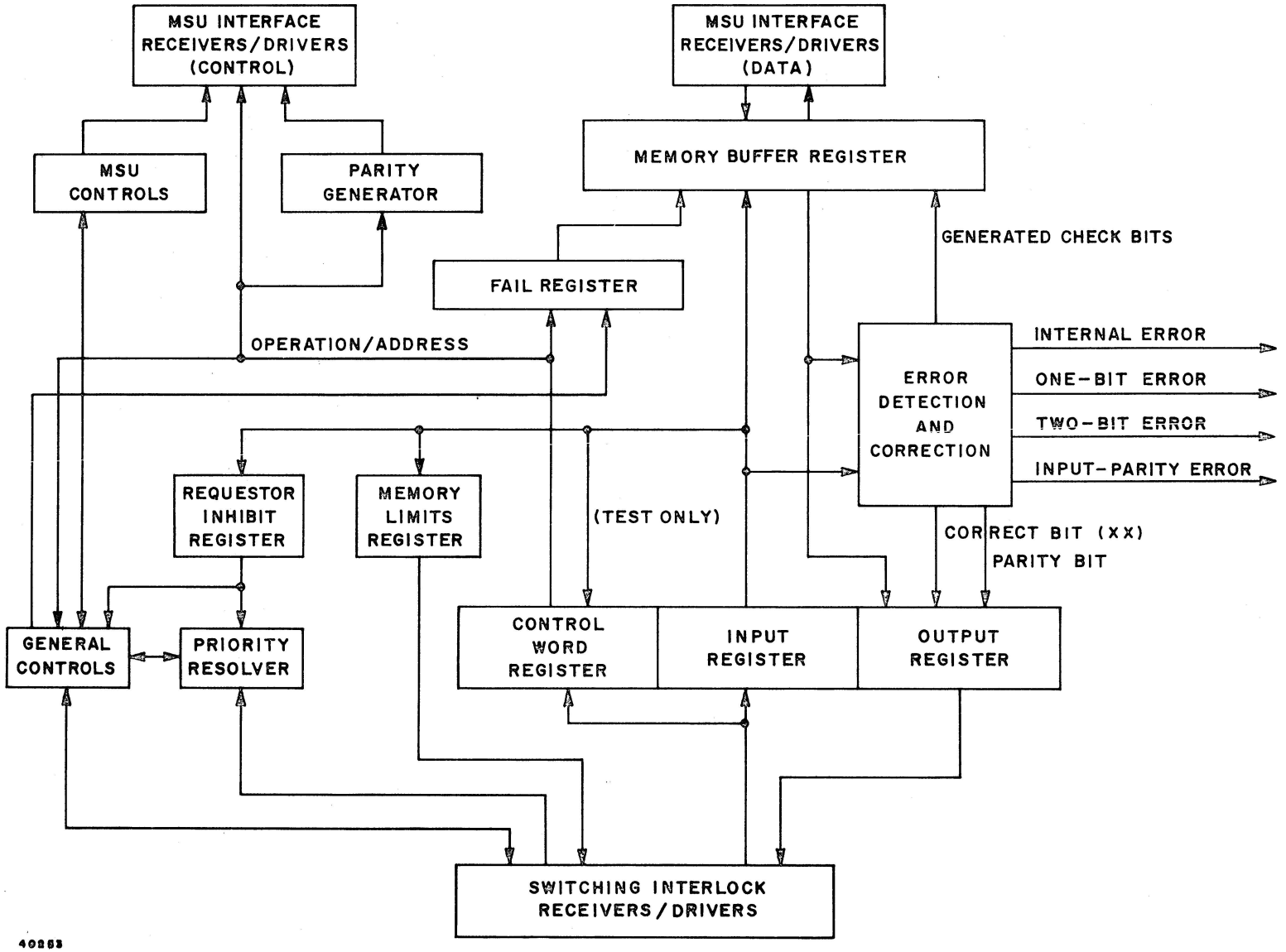


Figure V-2-1. Memory Control Module Block Diagram

The control word is stored in both the control word register and the input register. The general controls generate gating and timing pulses to transfer the control word from the input register to the error detection circuits to check for correct parity.

If a parity error is detected, the control word is transferred to the fail register, and a requestor operation-complete signal and a fail-interrupt signal are generated by the MCM and sent to the requestor. Also, if instructed by the requestor, the contents of the fail register are transferred to the requestor via the memory buffer register and output register. The parity bit for the fail word is generated in the error correction and detection circuits and applied to the fail word in the output register.

Assuming the control word contained no errors and was not a special request, the following process occurs:

a. The general controls circuits: generate necessary control pulses (such as requestors and set up timing, data timing, final read or write) for the operation to be performed; determine whether read or write operation to be performed; decode the word length of the operation and store it in the word count register if other than single word operation, and store the address residue of the control word for comparison with the address counter residue.

b. The MSU control: controls writing into and reading from the MSU; determines which MSU's are to be used; identifies the operation to be performed by the MSU (either read, or write, or read-modify write).

c. The parity generator: produces a parity bit for the 2-bit MSU operation plus the 16-bit address from the original control word before transfer to the MSU.

If the control word contained a write operation, the next input to the MCM is the data word (or group of data words as determined by the word length in the control word) from the requestor. The data word is placed in the input register which is the source of information for the error detection circuits. The error-detection circuits check incoming parity of the 52-bit word as received from the requestor and then generate seven check bits and an overall-parity for the entire 60-bit word. The 52-bit data word is transferred to the memory buffer register (MBR) where the seven check bits and the overall-parity bit are added to the data word. The 60-bit data word is then sent to the MSU for storage. This cycle is repeated for each data word written into memory.

If the control word contained a read operation, the 60-bit data word (or group of data words as determined by the word length in the control word) read from the addressed location or locations in the MSU is temporarily stored in the MBR. The data word is transferred to the error detection and correction circuits for comparison with the word as previously stored in the addressed location. The error-detection and correction circuits check for errors as the least significant 52-bits of the

data word are transferred to the register. If one of the bits was incorrect, the specific bit is corrected by complementing it in the output register. The correct data word is sent to the requestor together with a fail-2 interrupt signal which allows the requestor to record the error and also to continue processing with the correct data. If a 2-bit error occurs, the MCM sends a fail-1 interrupt signal to the requestor and loads the MCM fail register with the fail data.

If the control word is a special-request type (i.e., either "load requestor inhibit register" or "load memory limits register"), the general control circuits prepare for the transfer of the next data word directly from the input register (after parity check) to either the requestor-inhibit register or to the memory-limits register and MSU-available register located in the MSU controls. If the control word contains a "load requestor inhibit register" operation, the requestor inhibit register is loaded with new data to indicate which requestors now have access to the MCM. If the control word contains a "load memory limits register" operation, the MCM and MSU configuration is changed to reflect the number of MSU's available to the MCM as well as the upper and lower limits.

MCM FUNCTIONAL DETAILS

The functional details of the MCM are briefly presented here using the block diagram shown in Figure V-2-1.

Requestor Interface

The requestor interface contains the receiver/driver switch interlock logic which is used for all communications between the MCM and all requestors. Each requestor being serviced by an MCM contains these signal and data lines. The 52 information lines are used to transfer both the 52-bit data word and the 52-bit control word, both to and from the MCM. The remaining 26 lines are used to transmit control signals between the modules. Each of the 78 driver/receiver lines is a bidirectional driver/receiver but only 52 of these lines actually use the capability. The driver/receiver circuits are identical in all requestors and MCM's so that the receiver/driver circuit boards are interchangeable among the various modules. The receiver/driver logic for each of the 26 control signals is identical with the data lines; however the signals to enable the buffers are always present whenever power is up in the requestor and the MCM.

INFORMATION AND SIGNALS BETWEEN MCM AND REQUESTOR

The control and data flow between the MCM and the requestor is described in the following paragraphs.

1. Data and Parity - Data and parity are transferred between a requestor and an MCM via a unique set of 52-bidirectional data lines. These lines are also used for the transmssion of the control word. Odd parity is generated on all words transferred and the parity bit is transmitted in coincidence with the data.

2. Special-Request Signal (RQSN) - A special-request signal (RQSN) is used by a CPM to gain access to a memory con-

trol module (regardless of the state of the requestor-inhibits register) in order to load requestor inhibit(s) or memory limits. The RQSN signal goes "true" in coincidence with the request signal (REQ) and remains "true" until the receipt of an acknowledge signal (ACK) from the MCM.

3. Request Signal (REQN) - A request signal (REQN) is sent by a requestor to select a specific MCM. REQ goes "true" one clock period prior to the request strobe (RSTB) and remains "true" until the receipt of an acknowledge signal (ACK) from the MCM.

4. Data-Strobe Signal (DSTB) - A data-strobe signal (DSTB) is sent to inform the MCM that data is to be transmitted over the data lines. The signal is used only in the N-length overwrite and the N-word protected write operations. The data strobe precedes the data word by one clock and its width indicates the number of data words following it.

5. Request-Strobe Signal (RSTB) - A request-strobe signal (RSTB) is sent to inform the MCM that a control word is being transferred over the data lines. It is "true" initially one clock period following the start of the request signal (REQ). The control word is transmitted in coincidence with the request strobe.

   a. Single-word protected write and single-word overwrite: The request strobe (RSTB) will cycle "true" and "false" during successive clock periods. During the "false" period, the data word to be stored is placed on the data lines.

   b. All other operations: The request strobe (RSTB) is "true" one clock period following the request signal (REQN) and remains "true" until the acknowledge signal (ACK) is received.

6. Data-Available Signal (DAV) - A data-available signal (DAV) is transmitted to the requestor to indicate that data is available and may be transmitted in the following clock period. This signal goes "true" no earlier than one clock period before the data transfer and remains "true" no longer than requestor-operation-complete (ROC) time.

7. Acknowledge Signal (ACK) - An acknowledge signal (ACK) of one clock period duration is sent to the requestor to signify that the MCM has accepted the control word. This signal indicates to the requestor that he must terminate the transmission of the REQN and RSTB signals. It does not necessarily mean that the requested memory operation will be performed.

8. Send-Data Signal (SND) - A send-data signal (SND) is sent to the requestor during an N-length overwrite and may be sent during an N-word protected write. The send-data signal indicates the number of data words that must be trans-

mitted to the MCM. The number of words to be transmitted is equal to the number of clock periods the send-data signal is "true."

NOTE

The send data signal will not be transmitted if an attempt is made to write into a protected area during an N-word protected write. Also, the number of data words requested by the MCM must be transferred before a requestor ends his operation.

9. Data-Present Signal (DAPB) - Signal DAPB is sent to the requestor to indicate that a valid data word (or words) is being transmitted from the MCM. The DAPB is transmitted in coincidence with the data word. A word is transmitted each clock period that the DAPB is "true." The number of consecutive valid words being transmitted determines the width of the DAPB signal.

10. Requestor-Operation Complete Signal (RQOC) - The MCM sends a one-clock-period requestor-operation-complete signal (RQOC) to signify the end of the requestor's part of the memory operation.

The following variations apply:

a. Single or N-length fetches; single-word overwrite with flashback: The RQOC is sent coincident with the final clock period of the data-present signal (DAPB).

b. N-length overwrite; N-word protected write:

1. The RQOC signal is sent following the check of parity on the final data word received by the MCM for:

a. N-length overwrite

b. N-word protected write in which words were not protected.

2. The RQOC signal is sent with or following FALS signal if word(s) are protected in N-word protected write.

c. Single word overwrite without flashback: An RQOC is generated following the check of parity on the data word received by the MCM.

11. Address Upper Limit - The Address Upper Limit is the most significant six bits of the highest 20-bit memory access available to this MCM (the least significant 14 bits are assumed to be "1's").

12. Address Lower Limit - The Address Lower Limit is the most significant six bits of the lowest 20-bit memory address available to this MCM (the least significant 14 bits are assumed to be 0's).

13. Requestor-Enable Signal - The MCM sends to the requestor an enable signal which is used to enable or disable communications between the MCM and

the requestor. This signal is a steady-state signal which will disable communications:

1. Whenever the MCM is power cycling up or down.

2. Whenever the appropriate requestor inhibit FF is set.

14. MCM-Enable Signal - The requestor sends to the MCM an enable signal which is used to enable or disable communications between the requestor and the MCM. This signal is a steady-state signal which disables communications whenever the requestor is power cycling up or down.

15. Failure Interrupt 1 Signal (FAL1) - The MCM transmits a one-clock period FAIL 1 interrupt signal to the requestor if any of the following errors occur:

    1. Control word parity

    2. Illegal operation code

    3. Wrong MCM

    4. Data strobe error

    5. 2-bit error

    6. Internal error

    The MCM Fail Register will then be loaded with information to facilitate error analysis.

16. Failure Interrupt 2 Signal (FAL2) - The MCM transmits a one-clock period FAIL 2 interrupt to the requestor if a 1-bit error occurs. The MCM Fail Register will then be loaded with information to facilitate error analysis.

17. Software Interrupt (FALS) - A one-clock-period software error interrupt is transmitted to the requestor during a single-word or N-word protected write operation if the memory word being examined contains a "1" in bit 48. The FALS signal never occurs later in time than the requestor-operation-complete (RQOS) signal.

Priority Resolver

The function of the priority resolver in the MCM is to select the requesting channel to be serviced by the MCM. The order of servicing requestors (i.e., priority) is designed for maximum efficiency of a B 7700 System. Priority selection is based upon the lowest numbered requestor channel having the highest priority during simultaneous requests from a number of requestors. Priorities are hardwired so that in a system with 2 CPM's and 2 IOM's, the IOM's would be assigned priorities 0 and 1 and the CPM's would be assigned priorities 6 and 7. The priority resolver guarantees that a single high-priority requestor will not access memory with consecutive memory requests if a lower priority requestor has requested the memory. The priority resolver will enable/disable communications with the respective requestors as directed by the requestor inhibits except for CPM's using special requests. The special request bypasses the inhibit register check to provide either: load the requestor inhibit register, load the memory limits register, or fetch the fail register. The priority resolver will eliminate those

requestors from being serviced that have failed and could lock out other requestors.

Input Register

The input register is a 52-bit register that is used by the MCM to temporarily buffer both control words and data words received from a requestor. It is the source of data for the Memory Buffer Register, for checking the parity of the data word, and for the generation of the check-bits. During the initiation of an operation, a copy of the control word is loaded into the input register for parity checking.

The input from the requestor (either data word or control word) is transferred to the input register.

Depending on the transfer signals present at the output of the input register (IR), the IR bits are transferred to the memory buffer register (MBR), check bit generator and parity check circuits, memory limits register (MLR), or requestor inhibit register (RIH). If the information in the IR is either a control word, memory limits register (MLR) data, or requestor inhibit register (RIH) data, only a parity check is performed by the checker-generator circuits.

If the information in the IR is a 52-bit data word to be written into memory, the data is transferred to the memory buffer register during a write instruction and the data is sent simultaneously to the checker-generator circuits. The checker-generator circuits perform a parity check and also generate the eight check bits to make up the 60-bit data word for storage.

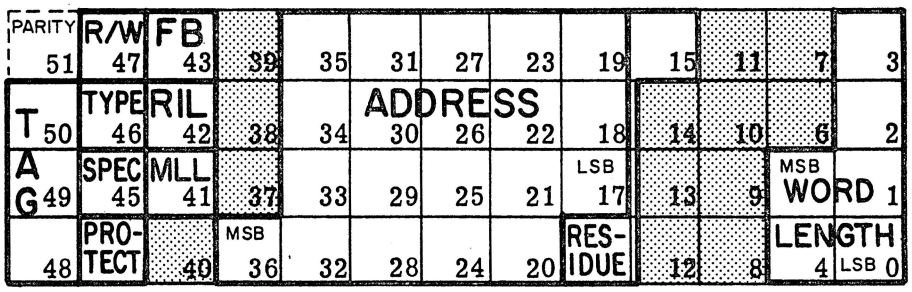
Control Word Register

The control word register is a 52-bit register in the MCM which is used to contain the control word transmitted by the requestor. The control word is transmitted from the requestor, follows the request signal by one clock, and is coincident with the request strobe. The control word format, bits, and fields as received at the CW register are as shown in figure V-2-2.

MCM Operational Characteristics

The MCM can be operated on-line during system operation or system test and off-line during module testing or maintenance.

All data transfers are word oriented. A word transferred between the MCM and a requestor contains the 48 bits of data, 3 tag bits, and 1 parity (odd) bit. Typical access and delay times for several operations are presented in Table V-2-1. Table V-2-2 lists the legal operation codes for the MCM.



Field	Bits	Description
PARITY	51:1	The reguestor generates a parity bit that will make odd parity for the 52-bit MCM CW.
TAG	50:3	In the MCM CW, the tag bits are examined for parity and are not examined for control purposes.
R/W	47:1	The R/W bit, when "0", specifies that a read/restore operation is to be performed. The R/W bit, when "1", specifies that one of the write variations (as further defined by the "type" bit) is to be performed.
TYPE	46:1	The "type" bit, when the R/W bit is a "1", specifies which write variation is to be performed. When the "type" bit is a "0", the clear/write operation is performed by the MSU. (The overwrite and the single-word protected-write operations use this variation. When the "type" bit is a "1", the read/modify/write operation is performed by the MSU. (The N-word protected-write operation uses this variation.) If the R/W bit is a "0" and the "type" bit is a "1", a fetch-the-fail-register operation is performed.
SPEC	45:1	The specifier bit, when a "1", indicates to the MCM that a single-word operation is to be performed. When the SPEC bit is a "0", an N-length operation is to be performed.
PROTECT	44:1	The protect bit, when a "1", indicates that a protected-write operation is to be performed. This bit must only be a "1" when doing a single-word protected-write operation or an N-word protected-write operation.

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Figure V-2-2. MCM Control Word Format (Sheet 1 of 2)

Field	Bits	Description
FB	43:1	The FB bit is used during the single-word overwrite operation and the single-word protected-write operation to specify that the original contents of the memory location are to be transmitted to the requestor.
RIL	42:1	The RIL bit is used with a single-word overwrite operation to specify that a load-requestor-inhibit operation is to be performed. When the RIL bit is a "1", the next data word is the requestor-inhibit field data word being transmitted to the MCM and will be loaded into the Requestor Inhibit Register instead of into the memory.
MLL	41:1	The MLL bit is used in a single-word overwrite operation to specify that the Memory Limit Registers (upper/lower/available) are to be loaded. When the MLL bit is a "1", the memory limits field of the next data word being transmitted to the MCM will be loaded into the Memory Limit Registers instead of into memory.
	40:4	Unused
ADDRESS	36:20	The address bits specify the word-starting address for this memory operation. The most significant six address bits are compared against pre-established address upper-limits and lower-limits in the MCM to determine whether the address to be accessed exists within the memory area assigned to this MCM.
RESIDUE	16:2	The address residue bits, bits 15 and 16, indicate the residue value of the 20-bit memory address within the control word.
	14:8	Unused
WORD LENGTH	5:6	The word length bits indicate the number of words to be transferred during N-length operations. The word-length field must never equal zero for any operation that is to be performed. In the case of single-word operations, the word-length field should equal a value of "1".

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Figure V-2-2. MCM Control Word Format (Sheet 2 of 2)

Table V-2-1. MCM Typical Times of Operation

OPERATION	REQUESTOR ACCESS	MCM BUSY TIME
Fetch (single)	1.750 usec	1.500 usec
Fetch (N-length) $0<N \leq 4$	1.625 + N (0.125) usec	1.375 + N (0.125) usec
Overwrite (single)	0.750 usec (CPM)* 0.500 usec (IOM) 0.500 usec (IOM)	1.500 usec
Overwrite (N-length) $N \leq 4$	1.125 + N(0.125)* usec (CPM) 0.500 + N(0.125) usec (IOM)	2.000 + N (0.125) usec
Single-word protected write/flash-back	1.750 usec	1.500 usec
Two-word protected write	2.125 usec (IOM only)	2.750 usec

* IOM completes access on Acknowledge (ACK) signal.
CPM completes access on Requestor Operation Complete (ROC) signal.

Table V-2-2. Legal Operation Codes for the MCM

Operation	MCM Control Word Bit 47	46	45	44	43	42	41
Single data word fetch	0	0	1	0	0	0	0
N-length data word fetch	0	0	0	0	0	0	0
Fail register fetch	0	1	1	0	0	0	0
Single-word overwrite with flashback	1	0	1	0	1	0	0
Single-word protected write	1	0	1	1	0	0	0
Single-word protected write with flashback	1	0	1	1	1	0	0
N-length overwrite	1	0	0	0	0	0	0
Single-word overwrite	1	0	1	0	0	0	0

Table V-2-2. Legal Operation Codes for the MCM (Cont'd)

Operation	MCM Control Word Bit 47	46	45	44	43	42	41
N-word protected write	1	1	0	1	0	0	0
Load requestor inhibits	1	0	1	0	0	1	0
Load memory limits	1	0	1	0	0	0	1

DEFINITION OF MCM OPERATIONS

The various MCM operations listed in table V-2-2 are briefly described here.

1. Data-Word Fetch (Single or N-Length) ($1 \geq N \geq 4$).

   This operation is a standard fetch of data. If an N-length fetch is initiated, the data words are transferred to the requestor at the clock rate, i.e., 125 nanoseconds, and within the limits discussed previously.

2. Fail-Word Fetch

   This operation is a fetch of the fail register within the MCM. The fail register is cleared as a result of this operation.

3. Single-Word Overwrite with Flashback

   This operation is a standard write/read operation. The data from the requestor is written into the addressed location. The original data read out of the address location is transferred back - or flashed back - to the requestor.

4. Single-Word Protected Write (with/without flashback)

   This operation is a conditional write of data into memory. The data word transferred by the requestor is written into memory only if the address is not protected (i.e., bit 48 of the original word is "0"). The requestor may indicate whether he requires flashback; however, the MCM will unconditionally flash back data to the requestor. The MCM will send a Fail S signal to the requestor if the address was protected.

5. Overwrite (Single or N-Word) ($1 \geq N \geq 4$)

   This operation is a standard write of data into memory. If the operation is an N-length overwrite, the rate of data transfer to the MCM will be controlled by the MCM.

6. N-Word Protected Write ($1 \geq N \geq 4$).

   This operation is a conditional write of data into memory. The data is written into memory as long as none of the addresses are protected (i.e., bit 48 = 0 for each address). The requestor will transmit the data only upon request of the MCM. The MCM will transmit a Fail S signal to the requestor if any of the addresses were protected, and it will unconditionally flashback data to the requestor.

7. Load Requestor Inhibit Register

   This operation is similar to a single-word overwrite with the exception that the data word is transferred to the requestor inhibit register instead of to the MSU. The state of the requestor inhibit register determines which requestors may communicate with the MCM.

8. Load Memory Limit

   This operation is similar to a single-word overwrite with the exception that the limits field within the data word is transferred to the memory limit register instead of to the MSU. The memory limits consist of the lower and upper MCM memory addresses and the MSU's available for usage by the MCM.

Requestor-Inhibit Register

The requestor-inhibit (RIH) register is an 8-bit register that is used by the MCM to hold the presently valid requestor inhibit. (See figure V-2-3.)

The output of this register is examined by the priority-resolution logic to determine which requestor or requestors are to be inhibited from gaining access to the MCM. Each output of the requestor inhibit register is handwired to one requestor so that, if his inhibit flip-flop is reset, the requestor who receives the encabling-level-present signal is allowed access to the MCM.

The outputs of this register are also transmitted to the requestors to enable/disable communications with them. A very important consideration is that this register is loaded programmatically by any central processor.

The requestor inhibit register is set by inputs from a requestor via the input register or by inputs from the MCM control panel or from the operator's console.

Memory Address Limits Register

The memory address limits register (MLR) is a 16-bit register made up of the following:

a. 6 bits to indicate the lower address limit. The lower address limit is the most significant 6 bit of the lowest 20-bit memory address available to this MCM (the least significant 14 bits are assumed to be "0's").

b. 6 bits to indicate the upper address limit. The upper address limit is the most significant 6 bits of the highest 20-bit memory address available to this MCM (the least significant 14 bits are assumed to be "1's").

c. 4 bits to indicate MSU availability

The address upper and lower limits define the addressing capability of this MCM within the total memory system. The MSU availability defines the MSU's available to this MCM which determines the maximum number of words of an N-length operation. These limits may be either programmatically loaded or loaded via the MCM Control Panel and Operator's Console switches. The MLR

PARITY 51	47	43	39	35	31	27	23	19	15	11	RI7 7	RI3 3
50	46	42	38	34	30	26	22	18	14	10	RI6 6	RI2 2
49	45	41	37	33	29	25	21	17	13	9	RI5 5	RI1 1
48	44	40	36	32	28	24	20	16	12	8	RI4 4	RIO 0

Field	Bits	Description
PARITY	51:1	The MCM examines the requestor inhibit word for odd parity.
	50:44	Unused
RI7	7:1	When bit RI7 is a "1", the requestor who is designated requestor 7 is inhibited from access to the MCM.
RI6	6:1	When bit RI6 is a "1", the requestor who is designated requestor 6 is inhibited from access to the MCM.
RI5	5:1	When bit RI5 is a "1", the requestor who is designated requestor 5 is inhibited from access to the MCM.
RI4	4:1	When bit RI4 is a "1", the requestor who is designated requestor 4 is inhibited from access to the MCM.
RI3	3:1	When bit RI3 is a "1", the requestor who is designated requestor 3 is inhibited from access to the MCM.
RI2	2:1	When bit RI2 is a "1", the requestor who is designated requestor 2 is inhibited from access to the MCM.
RI1	1:1	When bit RI1 is a "1", the requestor who is designated requestor 1 is inhibited from access to the mcm.
RIO	0;1	When bit RIO is a "1", the requestor who is designated requestor 0 is inhibited from access to the MCM.

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Figure V-2-3. Load Requestor Inhibit Word Format

data is established during initialization and is not changed unless reconfiguration of memory is necessary.

The 12-bits of lower and upper limits are cabled to all requestors' memory interface comparators. This information enables the requestor to relate the proper address with the proper MCM channel. The outputs of the 12 address bits (lower and upper limits) are compared with the six most-significant bits (CW36 thru CW31) of the requestor control-word address. If the control-word address is not within the lower and upper limits, a wrong address signal is sent to the fail word register which in turn sends a FAIL 1 interrupt to the requestor.

The outputs of the 6-bit lower limit and the 6-bit upper limit are hardwired to each requestor for comparison with pre-established memory limits for each requestor. If the requestor's memory operation address is within an MCM limit, the requestor initiates the request signal to access that MCM if the associated requestor inhibit (RIH) register bit is not set.

The output bits (1AV thru 4AV) are transferred to the memory controls to establish which MSU's are available to this MCM.

As with all flip-flops, the MDU and MCM panel have the capability of controlling and sensing the memory limit register.

The format of the memory address data word (as received in the IR following a load memory limits control word) is shown in figure V-2-4.

Memory Buffer Register

The memory buffer register (MBR) is a 60-bit register that is used by the MCM as a temporary buffer register for data words transferred to or from MSU's. The input sources to the MBR (for the data transfers to an MSU) are: the input register for the least significant 52 bits (bits 00 thru 51), the error-code check bits (bits 52 thru 58), and the overall parity bit (bit 59). The input source to the MBR for data transfers from the MSUs is from the MSU interface receiver/drivers. The MBR is the source of data for the error-code checking logic to determine if bit correction is necessary for words transferred from an MSU to the MCM.

During a fetch the fail-register operation, the fail register information, except bit FR51, is transferred to the MBR before being placed in the output register.

Failure Interrupt Signals

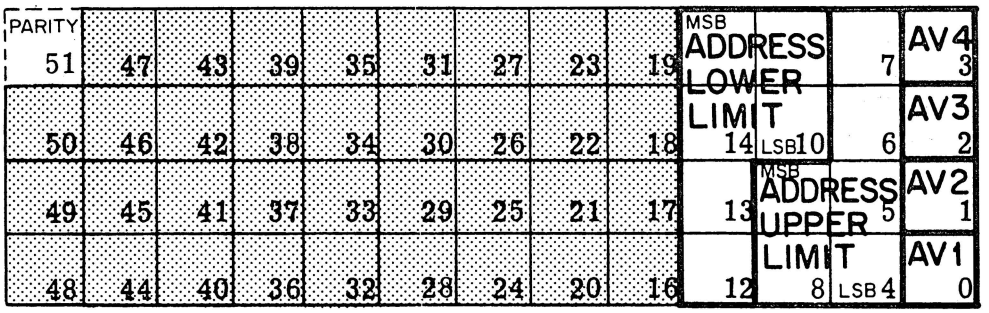
The error controls, detection, and correction logic use three failure interrupt signals: Fail 1, Fail 2, and Fail S.

FAIL 1 INTERRUPT SIGNAL

The Fail 1 interrupt is generated and sent to the requestor when an irrecoverable error has occurred even though the requestor memory operation may not be completed. The fail register is loaded with the information listed below to facilitate failure analysis:

a. R/W Bit

b. MSU Availability



Field	Bits	Description
PARITY	51:1	The MCM examines the memory address limits word for odd parity.
	50:35	Unused
ALL	15:6	The address lower limit is the most significant 6 bits of the lowest 20-bit memory address available to this MCM.
AUL	9:6	The address upper limit is the most significant 6 bits of the highest 20-bit memory address available to this MCM.
AV4	3:1	When AV4 is a "1", the MSU designated MSU4 is available to this MCM.
AV3	2:1	When AV3 is a "1", the MSU designated MSU3 is available to this MCM.
AV2	1:1	When AV2 is a "1", the MSU designated MSU2 is available to this MCM.
AV1	0;1	When AV1 is a "1", the MSU designated MSU1 is available to this MCM.

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Figure V-2-4. Memory Address Limits Word Format

c. MCM Number

d. Requestor Channel Number

e. Error Type

f. Error Address

Requestor operations will always be completed when the following errors are detected:

a. Two-Bit Error (fetch only)

b. Checker/Generator Error

c. Address Failure

d. Data Word Parity Error

Requestor operations will never be completed when the following errors are detected:

a. Control Word Parity Error

b. Illegal Operation

c. Wrong Address

d. MSU Parity Error

e. Read Available Failure

f. Two-Bit Error (protected write)

g. Data Strobe Error

h. MSU Unavailable

Requestor operations may or may not be completed when the following errors are detected within the MCM:

a. Parity Generator (MSU control) Failure

b. Data Timer Failure

c. Data Transfer Control Failure

d. MSU Availability Error

NOTE

The Fail 1 interrupt signal is transmitted to the next requestor for any internal error detected during or after requestor-operation-complete time. A checker/generator error is an exception in that the Fail 1 signal is sent to the original requestor. Within the fail register the R/W bit and requestor channel number belong to the first requestor, and bit 48 of the fail register is set to indicate that this was a delayed-interrupt situation.

FAIL 2 INTERRUPT SIGNAL

The Fail 2 interrupt is generated if a one-bit error has occurred. When a Fail 2 signal is sent to the requestor, the following information is loaded into the fail register:

a. Error Bit Number

b. Error Address

c. Error Type (one-bit)

FAIL S INTERRUPT SIGNAL

The Fail S interrupt is generated if a protected word was found during a protected-write operation. The Fail S signal is sent to the requestor, but no error indications are recorded in the fail register.

Fail Register

The fail register is a 52-bit (FR51-FR00) register used to contain all pertinent information necessary to identify and define a failure. The fail information remains in the fail register until a fetch-the-fail-register operation request is made by the requestor or a clear operation is performed. During a fetch-the-fail-register operation, the information is returned to the requestor through the memory buffer register (MBR) and output register. Word parity for the fail word is generated in the parity generation logic and added to the fail word in the output register before transfer to the requestor.

The format, bits, and fields of the MCM fail word are illustrated in figure V-2-5.

Error Detection and Correction

The MCM uses the memory buffer register (MBR) as the source of data for the error-code checking logic which determines if bit correction is necessary for words transferred from an MSU to the MCM. The MBR and the logic cards are located in the MCM. The functional logic of error detection and correction is illustrated in figure V-2-6 and briefly described in the following paragraphs.

The horizontal row of numbers shown in figure V-2-6 indicates the bit positions within the 60-bit stack word. The format of a word transferred between an MCM and a requestor is: bit 00 thru bit 47 are data bits (providing for six EBCDIC characters, or eight BCL characters, or 12 digits, etc.), bits 48 thru 50 are tag bits (for word control), and bit 51 is a parity bit (odd parity is correct parity) for bits 00 thru 51. Bits 52 thru 59 are not transmitted from an MCM to a requestor. Bits 52 thru 58 are called check bits and bit 59 is an overall-parity bit (the correct parity is odd parity) for the 60-bit stack word.

Each horizontal row of X's represents a mask used in generating the check bits. The bit positions which are used in generating a check bit for a particular mask are indicated by the X's. Altogether, there are seven different masks.

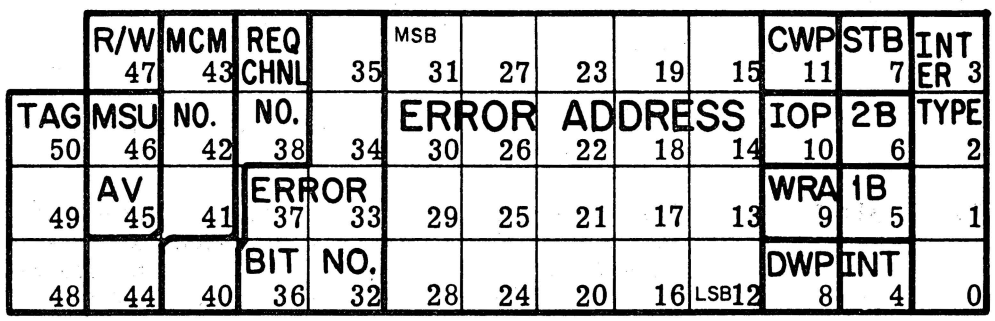
Using each of the seven masks, the bit indicated by the X in the check-bit field is set or reset so as to generate even parity for that set of bits. For example, using the group 1 mask if bit 01 was set and bit 02 thru bit 51 and bit 00 were reset, then bit 1 in the check-bit field would be set to give even parity for the bits considered.

It should also be pointed out that the overall-parity bit (bit 59) is set or reset to give odd parity for all bits in the 60-bit word, including the check bits.

As each word is retrieved from the MSU, the MCM checks the overall-word parity and again applies the seven masks to determine if one or more bits have been altered. The MCM detects two basic types of errors.

a. One-bit errors

   A single-bit error, whether a drop-out or pick-up, is de-



Field	Bits	Description
TAG	50:3	If the delayed-interrupt bit (bit 48) is set it indicates that the MCM has detected an internal error during or after the requestor-operation complete (ROC) flip-flop has been set. The interrupt signal is saved until the next requestor's operation for delayed interrupt reporting.
R/W	47:1	The R/W bit indicates when the error is detected whether the operation being executed was a read operation or a write operation.
MSU AV	46:2	The MSU AV field indicates which MSU(s) is available to this MCM. The field interpretation is:
MCM NO.	44:4	The MCM number is a preassigned number (from 0 thru 15) that is placed in the MCM-number field of the fail word to identify the specific MCM with the error condition.
REQ CHNL NO.	40:3	The requestor-channel-number field contains the number of the requestor who was communicating with the MCM when the fail register was loaded (except when a one-bit error detection and correction occurs, in which case, the field contains the number of the requestor who is fetching the fail register).

Bit 46	Bit 45	
0	0	No MSU is available
0	1	One MSU is available
1	0	Two MSU's are available
1	1	Four MSU's are available

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Figure V-2-5. MCM Fail Word Format (Sheet 1 of 3)

Field	Bit	Description
ER BIT NO.	37:6	If a one-bit error occurs, the binary number of the bit that failed is placed in the error-bit-number field.
ER ADDRS	31:20	The error-address field contains the address of the location that was being accessed if a one-bit or two-bit error occurred. The address is related to one-bit or two-bit errors as follows:

Error Indication 2-Bit	Error Indication 1-Bit	Error Address Belongs to:
0	1	1-Bit Error
1	0	2-Bit Error
1	1	1-Bit Error

CWP	11:1	When the CWP bit is a "1", incorrect control-word parity is indicated.
IOP	10:1	When the IOP bit is a "1", the operation specified by the control word that caused the error was an illegal-operation code. (Refer to Table V-2-2) or one of the following errors is indicated: (1) Word length = 0 (2) For single-word operations word length >1 (3) For requestor-inhibit load or memory-limits load the special-request strobe is absent.
WRA	9:1	When WRA (wrong address) bit is set, it indicates that the six most-significant bits of the address in the control word did not fall within the address limits assigned to this MCM.
DWP	8:1	A data-word parity (DWP) error indicates a data word containing even parity was received from the requestor during a write operation.
STB	7:1	A data-strobe (STB) error indicates that either too many or too few data strobes were received by the MCM during an N-length overwrite or an N-length protected-write operation.
2B	6:1	A 2-bit (2B) error indicates that two bits were found in error during error checking of a data word as it was read out of memory.

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Figure V-2-5. MCM Fail Word Format (Sheet 2 of 3)

Field	Bits	Description
1B	5:1	A 1-bit (1B) error indicates that a single bit was found in error during error checking of a data word as it was read out of memory.
INT	4:1	The internal-error (INT) bit indicates that a logic failure occurred within the MCM or MSU. Bits 0 thru 3 in the fail word register must be examined to determine the type of error.
INT ER TYPE	3:4	If the internal-error bit is a "1", these bits will contain a code indicating the nature of the failure. The codes listed define the errors.

Fail Word Register Bits (3 2 1 0)	Indicated Error Type
0 0 0 0	MSU Unavailable
0 0 0 1	Read Available Error
0 0 1 0	Checker/Generator Error
0 0 1 1	Address Counter Failure
0 1 0 0	MSU Address Error
0 1 0 1	Parity Generator (MSU Control) Failure
0 1 1 0	Data Timer Failure
0 1 1 1	Data Transfer Control (DTC) Failure
1 0 0 0	MSU Availability Error

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Figure V-2-5. MCM Fail Word Format (Sheet 3 of 3)

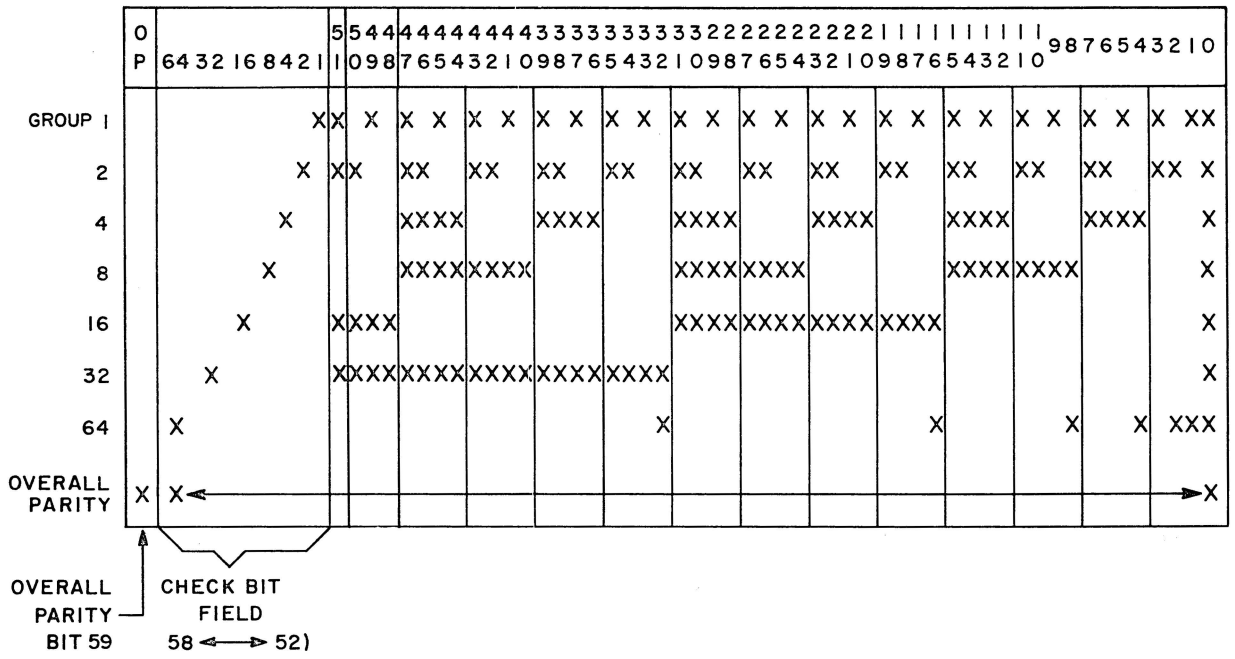


Figure V-2-6. Bit Positions for Error Detection and Correction

tected and corrected. One-bit errors are detected by an indication of bad overall parity and the presence of one or more group errors. The bit with erroneous parity is isolated and corrected in the MCM output register.

b. Two-bit errors

Two bit errors are detected by an indication of good overall parity and the presence of one or more group errors. There is no automatic correction for two parity bit errors.

A single-bit error in the 59-bit word is detected by the parity check on the overall word. The check bits generated by again applying the error detection masks give the position of the bit in error. The MCP would be notified that an error had occurred, but the corrected word would be available for use. The MCP would log the error for maintenance purposes and allow processing to continue.

If two bits of the 60-bit word are in error, the overall-word parity check will not indicate an error. In this case, the checking operation will indicate the presence of one or more group errors. The information cannot locate the position of the error but is used to indicate the existence of an error. More than two bits in error may appear either as a single-bit error, as a two-bit error, or as no error.

In summary, 1-bit errors are detected and corrected 100% of the time. Error correction of 1-bit errors requires 3 MCM clock pulses, i.e., 375

nanoseconds. Two-bit errors are detected and multiple even-bit errors may be detected, but neither are corrected. When multiple odd-bit errors are detected, one bit is corrected and the data is transferred to the requestor (A parity check may show that an error still exists.).

A failure which indicates both odd and even parity errors while checking or generating the parity of the respective groups is identified as a hardware failure of the check/generator logic itself.

Output Register

The output register is a 52-bit (OR00-OR51) register used to buffer data words (includes fail data) that are being transmitted to a requestor during a fetch operation. The output register also contains the bit-correction logic required to correct one-bit errors detected by the error-correction logic.

The basic input for the output register is from the memory buffer register which contains data transferred from memory storage. Bit correction for one-bit errors is accomplished after the output register is loaded from the MBR.

The output of the output register is transferred to the requestor via the switching interlock driver/receivers.

MSU Control

The MSU control is used for: routing control signals and addresses to the correct MSU; read or write (including all variations) timing; and address conversion required for the various MSU configurations.

MCM-MSU Control and Data Interface

The MCM-MSU interface contains the receiver and driver line buffers which provide interconnection logic levels for control and data flow.

Master Clock and System Distribution

The master clock for a B 7700 System is housed in the MCM cabinet designated MCM-0. Although all MCM's are so configured that they could house the master clock kit, only one master clock is used per system.

The master clock consists of three circuit cards: the crystal-controlled master clock, 2MHz countdown, and crystal-controlled 5MHz clock. The crystal-controlled master clock provides three outputs consisting of the following: a 16MHz signal which is supplied to the CPM's as the clock signal for the program control unit, storage unit, and execution unit; an 8MHz phase-1 signal which is supplied to the CPM's (communications unit only), IOM's, and MDU's as the basic clock signal for internal and interface timing; and an 8MHz phase-2 signal which is supplied to all MCM's as the basic clock signal for internal and interface timing. The 2MHz countdown circuit card steps down the 8MHz phase-1 signal to provide a 2MHz clock signal for the disk file optimizer (DFO). (The DFO does not contain an internal clock generator.) The 5MHz crystal-controlled oscillator provides the clock signal for the data communications processor.

The master clock system obtains its dc input power from special power supplies that are isolated from the normal power supplies in each module. Therefore, if the MCM containing the master clock is shut down, the master clock will continue to drive the other MCM's and system modules.

SECTION 3
MEMORY STORAGE UNIT

GENERAL DESCRIPTION OF MSU

The memory storage unit (MSU) of the B 7700 is a coincident current random access, magnetic core storage device that uses the memory control module (MCM) as its interface with the B 7700 system requestors (IOM and CPM). Each MCM can control a maximum of four MSU's. The number of MSU's contained in a B 7700 system is determined by the amount of memory storage required for the particular application.

The MSU stores information in a core memory stack and has the capability of presenting this information upon request. All inputs and outputs to a MSU are controlled by the MCM assigned to that particular MSU. Therefore, all requestor operation requests (that require a memory module) first go to an MCM before being processed by an MSU. The interface control signals and data signals used between the MSU and MCM are shown in figure V-1-3.

The MSU contains the necessary storage elements, driving and sensing circuitry, address and data registers (read and write), control timing and decoding, power and interface logic necessary to perform the required operations.

MSU FUNCTIONAL DESCRIPTION

The B 7700 memory storage unit (MSU) is divided into two functional areas: the memory logic module (MLM) and the memory storage module (MSM).

The function of the MLM is parity checking, timing, and control, and to provide those conversion logic circuits required to interface between the memory control module (MCM) and the MSM. A basic function of the MLM is to make the MCM logic levels compatible with the MSM logic levels. Since the MCM is designed with CTL logic circuits and the MSM is designed with TTL logic circuits, the logic circuit signal levels must be converted from CTL to TTL (MCM to MSM) and from TTL to CTL (MSM to MCM) via buffer stages contained in the MLM.

The MSM contains: the 65,536 60-bit word core memory; the read information register; associated address decoding logic; read and write drivers; and timing and control logic.

There are three operational modes provided by the MSU: read/restore, clear/write, and read/modify/write. The cycle time of a single operation is 1.5 microseconds, while the read access time is 0.7 microseconds.

1. Read/Restore

   The MSU reads out data from the memory address defined by the MCM and places the data on the bus to the MCM. The MSU rewrites the information back into the core memory at the defined address.

   The following MCM operations use this MSU operation:

   a. Single-word fetch

   b. N-length word fetch

2. Clear/Write

   The MSU reads out data from the memory location addressed by the MCM and places the data on the bus to the MCM. The MSU accepts information from the MCM and stores it into the addressed location.

   The following MCM operations use this MSU operation:

   a. Single-word overwrite with or without flashback.

   b. N-length overwrite.

   c. Single-word protected write.

3. Read/Modify/Write

   The MSU reads out data from the memory location addressed by the MCM and places the information on the bus to the MCM. The MSU on command from the MCM, stores into the same address either the original information read from memory or information transmitted from the MCM.

   The N-word protected write uses this MSU operation.

There are three registers in the memory storage cabinet:

MEMORY ADDRESS REGISTER (MAR)

The MAR is a 16-bit register that is used by the MSU to identify the core stack location into which or from which the information (60 bits) is to be stored or fetched.

MEMORY WRITE REGISTER (MWR)

The MWR is a 60-bit register that is used by an MSU to buffer information from the MCM that is to be written into a stack location.

MEMORY READ REGISTER (MRR)

The MRR is a 60-bit register that is used to buffer information to be transferred to the MCM from a stack location. The MRR is also used as a source of write data during the N-length protected write if the word is protected.

An MSU has 65,536 address locations, each with 60 bits of storage available. Of these 60 bits, 48 are data bits, 3 are tag bits, 1 is a parity bit for the requestor's word, 7 bits are for error detection, and 1 bit is for overall parity for the word while it is in the memory module. The error-check bits and the overall parity bit are sufficient to detect one-bit failures throughout the 60-bit field. Whenever information is stored in memory, these error check bits and the overall parity bit are set according to the new information within the stack word. Only the 48 data bits, 3 tag bits, and 1 parity bit are transferred to a requestor.

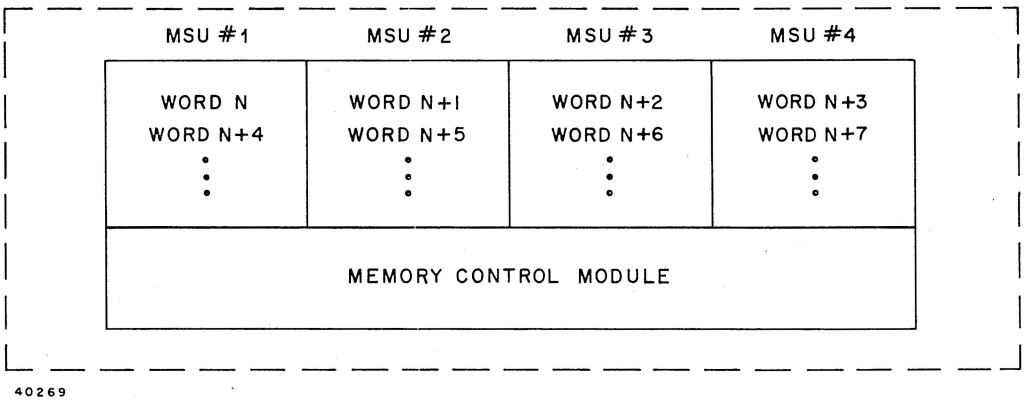


Figure V-3-1. Interlacing MSU's

Memory Interlacing and Phasing

A large percentage of memory operations consists of transferring several words to or from consecutive memory locations. If consecutive memory locations within a memory storage unit are accessed, the transfer rate is restricted by the cycle time of the memory storage unit. This results in reduced efficiency of the requesting module which may be forced to wait for transfer of information from memory.

This restriction may be alleviated by assigning memory addresses in such a way that consecutive addresses fall in different memory storage units. (See figure V-3-1.) This allows a second MSU to prepare for a memory cycle while the first MSU is transferring a word, and the second MSU to transfer a word while the first MSU is completing its cycle. This procedure is known as interlacing.

A 4-MSU memory module may be interlaced in such a way that four consecutive addresses fall in four different memory storage units. The effect is that multiple-word transfers (phasing) occur in bursts of four words each, one at each successive clock. A 2-MSU memory module may be interlaced so that bursts of two words can be obtained.

CHAPTER VI
FAILSOFT AND MAINTENANCE

The B 7700 system embodies two principles of fail-soft design: first, each module of the system is very reliable and, second, the system as a whole can continue to function despite failures in individual modules. To this end, the basic objectives of fail-soft design have been not only to provide for the immediate detection and isolation of any failure but also to make each function of the system available by means of more than one system resource.

Stated in terms more congenial to a user of the system, the primary goal of B 7700 fail soft is to keep the system running 100 percent of the time. Related closely to this goal there are two others: to minimize system degradation and to provide the user with tools for performing his own data recovery. Together, the three goals of B 7700 fail-soft design are achieved by a combination of hardware and software facilities throughout the system.

The first goal--to keep running--accomplished as follows:

1. By the high reliability of system hardware.
2. By the incorporation of error detection circuits throughout the system.
3. By single-bit error correction of errors in memory.
4. By recording errors for software analysis.
5. By modular design, by use of separate power supplies and redundant regulators for each module, and by use of redundant buses.
6. By the ability of the master control program to automatically reconfigure the modules of the system to temporarily exclude a faulty one.

Although the capability to reconfigure the system upon the isolation of a defective module is primarily a function of the Master Control Program, there are features built into the hardware that aid the software. For example, four interrupt management levels, or machine modes of operation, are used to provide three complete changes of environment in instances of repeated interrupts. These features allow the Master Control Program to seek a failure-free environment in which recovery tasks (logging of the failure, isolation of jobs affected by the detected error, system reconfiguration, and restarting of users' jobs not affected by the failure) can be carried on.

In short, the detection and reporting of errors is done by hardware, analysis of errors is done by software, and the reconfiguration of the system is done dynamically by software. Because of the modularity of the system and the redundancy of interconnecting buses, a failure of a single module or of a single connection will not totally disable the system. Moreover, because of the modularity of power supplies and the use of redundant regulated supplies

for critical voltages, the impact of a malfunctioning dc supply is minimized and does not result in a catastrophic failure.

The second goal--to minimize system degradation--is achieved by providing diagnostic programs and equipment for rapidly identifying and repairing faults and for reestablishing confidence in a repaired module before it is returned to the user's system. The diagnostic programs of the B 7700 system identify a faulty module on line. By the off-line use of the maintenance diagnostic unit, a fault in any main-frame module or in a disk file optimizer is narrowed to a single clock period and to a flip-flop and its associated logical circuits. Finally, by the use of the card tester on the maintenance diagnostic unit, the faulty integrated circuit chip is identified.

The third goal--to provide the user with tools for performing his own data recovery--is achieved by the use of such features as installation allocated disk, protected disk files, duplicated disk files, and fault statements in the high-level programming languages used on the system.

The remainder of this chapter summarizes the high points of the B 7700 fail-soft and maintenance design, as follows:

1. The immediate detection, reporting, and correction of errors.

2. The independence of main-frame modules.

3. The rapid identification and repair of faults.

4. Data recovery techniques.

DETECTION, REPORTING, AND CORRECTION OF ERRORS

Extensive error checking facilities allow for the immediate detection of a failure--a basic premise of fail-soft design. This feature is combined with the reporting of errors in the fail registers of the central components of the system and with the correction of single-bit errors in memory.

Detection and Reporting of Errors In the CPM

The use of residue checking in all arithmetic operations and of parity checking and continuity checking in data transfers greatly facilitates the detection of errors within the central processor module. If a failure occurs within the central processor module, a processor internal interrupt is produced and the cause of the failure is denoted by the contents of the fail register of the processor.

Within the execution unit (EU) of the central processor module, parity is used to detect errors in EU local storage and in data received from other units. Mod 3 residue checking is used to detect errors anywhere in the EU data paths and data registers, particularly in the adder and in the barrel register, but not in the EU local storage or control registers. Also, residue checks are made on addresses sent to the EU from the address unit, and residue is supplied for addresses sent by the EU to the address unit or storage unit. In addition, residue checking is the primary means of detecting an error caused by an extra data transfer signal. Continuity

checking, the use of a validity bit that indicates whether or not the current contents of a register are valid, is used to detect missing and sometimes extra data transfer signals for the most commonly used EU data paths.

Detection and Reporting of Errors in the IOM

There are facilities for detecting errors that may occur in any operation in which data are transferred into or out of the system. Among the error detecting features of the input/output module are parity checking of data transfers, residue checking of all arithmetic operations, parity checking of all local memory operations, timeout on memory transfers and scan bus operations, memory bounds checking, detection of illegal commands and conditions, and parity checking of register-to-register transfers.

Particular care is taken in addressing main memory: residue checks are made in the calculation of memory addresses, and bounds checks are made each time an attempt is made to gain access to main memory.

When a failure occurs in an input/output subsystem, it is reported in a result descriptor which pinpoints the fault. Failures are reported in two distinct ways; if a failure can be associated with an I/O operation, such as a parity error on magnetic tape, the failure is reported with the normal I/O complete information for that unit and further automatic processing of additional I/O requests for that unit by the IOM is inhibited. A channel interrupt can be triggered on an I/O Termination operation if requested by software. A failure which is not associated with a specific I/O request is reported in a special format "fail" result descriptor, and an IOM error interrupt is sent to the MCP.

Detection and Correction of Single-Bit Errors in Memory

All single-bit memory errors are detected and corrected; the fail register of the memory control module is loaded with information about the failure, and the requestor (central processor module or input/output module) is notified of the failure (an interrupt is generated) and of the type of error that occurred. The ability of the memory control module to perform single-bit error correction not only greatly increases availability but, more important, also eliminates a source of transient errors which persist until a pattern has been established. In the B 7700 system the transient errors are corrected, and the log of fail register contents provides the information for establishing the failure pattern.

Detection and Reporting of Two-Bit Errors in Memory

Two-bit errors are detected and reported but not corrected. Again, the fail register of the memory control module is loaded with information about the failure, and the requestor is notified of the failure (a fail 1 interrupt is generated) and of the type of error that occurred. (A fail 1 interrupt is always generated when an irrecoverable memory error occurs.)

INDEPENDENCE OF MODULES

To effectively make use of the error detection capabilities just dis-

cussed, isolation of errors is necessary. Achieving this isolation of errors involves not only the logical organization of system modules and interfaces but also the logical organization of system modules and interfaces but also the physical redundancy of modules and cables and the isolation of modules. Logical features, such as redundant module address selection for intermodule communication, are useless if a single connection failure can disable all intermodule traffic. Hence, the B 7700 intermodule cabling and the power distribution are designed to preserve module independence. The independence of main-frame modules is accomplished by use of a distributed switching interlock and by a distributed fail-soft power subsystem.

Distributed Switching Interlock

In any system which requires redundant processors to provide sufficient system availability, several interface problems must be solved:

1. How does one processor know that the other processor is inoperative; how long after failure does this knowledge become available?
2. How is current information maintained available to both processors?
3. How are in-process I/O operations terminated in an orderly fashion?

These questions are answered very simply on the B 7700 system, since the distributed switching interlock interconnects all main frame modules. The switching interlock does not exist as a single entity but is distributed among the main frame components and thus does not rely on any one component for its operation. The central processor and input/output modules are treated as requestors and each module has a unique path to each of the memory modules. Priority resolution logic in each of the memory control modules ensures that each requestor is served. There is, in addition, an access mask in each memory control module, which may be set by software. This feature enables the system to be divided into several systems, but, more important, it provides the ability to lock out suspect or faulty requestors (central processor and input/output modules) from memory modules containing operational programs and data base.

The interface problems between main frame components are readily solved, because all main frame components are interconnected. Communication between processors is easily maintained by the use of interrupts and shared memory. Since all information is available to all processors, processor may initiate input/output requests and respond to the termination of an input/output operation.

Distributed Fail-Soft Power Subsystem

The power subsystem of the B 7700 system is characterized by the modularity of power regulators, the location of individual power supplies and regulators in each cabinet of the central B 7700 system, and the parallel operation and redundancy of power regulators.

The true test of a modular fail-soft system is whether it is possible to perform maintenance on a module without interfering with other modules. Hence, in the B 7700 system, power supplies are distributed so that power sequencing in one module does not interfere with another module. Not only do the central components of the system have separate power supplies and regulators, but critical power supplies are duplicated within each module.

Because the cabinet of each central component of the system has its own individual power supplies and regulators, a power failure in one cabinet has no effect on the power supplied to other modules of the system. Ac power is brought to the cabinet of each central component, where it is converted to a 160-volt dc level--the base input to the power regulators (-12 volt, -6 volt, 4.8-volt, and -2 volt) in the cabinet. The modular power regulators are easily removed and replaced.

An optional fail-soft feature, redundant power regulators work in parallel with each other; if one should fail, the other immediately assumes the full load. Redundant power kits (for both -2 volt and 4.8-volt power) are available for each of the following central components: the central processor module, the input/output module, the memory control module, and the maintenance diagnostic unit.

The power subsystem also provides overvoltage and undervoltage protection for direct current, overvoltage protection for alternating current, and current regulation.

IDENTIFICATION AND REPAIR OF FAULTS

The rapid identification and repair of faults is done by use of confidence and diagnostic programs and by the use of the module and card testing facilities of the maintenance diagnostic unit.

Confidence and Diagnostic Programs

Both on-line and stand-alone confidence and diagnostic programs for both the central components of the B 7700 system and peripheral devices are provided as standard B 7700 system software. In addition, test tapes used with the maintenance diagnostic unit are provided for the off-line testing of the central processor module, the input/output module, the memory control module, and the disk file optimizer.

Maintenance Diagnostic Unit

The maintenance diagnostic unit is a console that in conjunction with a dedicated magnetic tape unit is used in off-line testing of the central processor module, the input/output module, the memory control module, and the disk file optimizer, and in testing the cards of these components of the system. When by the use of on-line confidence and diagnostic programs a faulty module has been identified, the cause of the trouble is further traced first to the card level and finally to the circuit level by the use of module testing and card testing facilities of the maintenance diagnostic unit.

The maintenance diagnostic unit is permanently connected by dedicated cables to all modules that can be tested. Tests are initiated from the dedicated magnetic tape unit or manually from the panels of the

maintenance diagnostic unit. Selectable test options provide for stopping on an error or cycling.

Because the modules that it tests have logical circuits dedicated to maintenance, the maintenance diagnostic unit is capable of controlling (setting, and resetting) and sampling all of the flip-flops of these modules. The maintenance diagnostic unit controls the clock of the module under test; single clock pulses and trains of clock pulses can be used.

The strategy of testing modules on the maintenance diagnostic unit is to exercise a faulty module and clock period by clock period to compare the states of its flip-flops with a prerecorded norm. In this way a trouble is traced to a clock period and to a flip-flop and its associated logical circuits. Similarly, the testing of faulty cards on the card tester of the maintenance diagnostic unit is carried out by providing input patterns to a card, sampling its outputs, and comparing them with predetermined norms.

DATA RECOVERY

Installation allocated disk allows the user to specify the physical allocation of his critical disk files in order to facilitate the maintenance and reconstruction of these files. Protected disk files allow a user to gain access to the last portion of valid data written in a file before an unexpected system halt. The use of duplicated disk files is to avoid the problem of fatal disk file errors. The master control program maintains more than one copy of each disk file row, and, if access cannot be gained to a record, an attempt is made to gain access to a copy of the record. By the use of fault statements, the user can stipulate the actions to be taken by his programs in case certain errors occur.

CHAPTER VII
CONTROLS AND INDICATORS

SECTION 1
OPERATING CONTROLS

INTRODUCTION

This section describes the controls and indicators used in the operation of the B 7700 system. These controls and indicators are located on the operators control console and on the cold start/halt load selection cards. The operators control console (figure VII-1-1) consists of a console control panel and one or more supervisory console devices, each of which contains an input keyboard and a video output screen. The cold start/halt load selection cards are mounted in the backplane of each CPM and IOM.

CONSOLE CONTROL PANEL

The console control panel (figure VII-1-2) includes the following switches and indicators.

SYSTEM A/SYSTEM B - This switch selects the portion of the system which will be affected by the remaining switches on the console control panel. Each main frame module (CPM's, IOM's, and MCM's) includes a SYSTEM A/SYSTEM B switch which determines which portion of the system that module belongs to. Only those mainframe modules belonging to the selected portion of the system are affected by operation of the console control panel switches.

The SYSTEM A/SYSTEM B switch is located on a switch card (the COLD START/HALT LOAD selection card) mounted on the backplane of a CPM or IOM. The SYSTEM A/SYSTEM B switch is mounted on the cabinet frame at the right side of the panel of an MCM.

HALT LOAD/COLD START - This switch selects the load operation that will be performed when the system is started.

When set to COLD START, indicate that a card load has been selected.

When set to HALT LOAD, indicates that a disk load has been selected.

Note that this switch selects the mode of operation, but does not cause the operation.

HALT - Halts the system in an orderly fashion. Sets CPM's to single instruct mode, which causes a halt at the end of the current program operator, and sets IOM's to inhibit state, which inhibits the initiation of further I/O operations. I/O operations in progress will be completed.

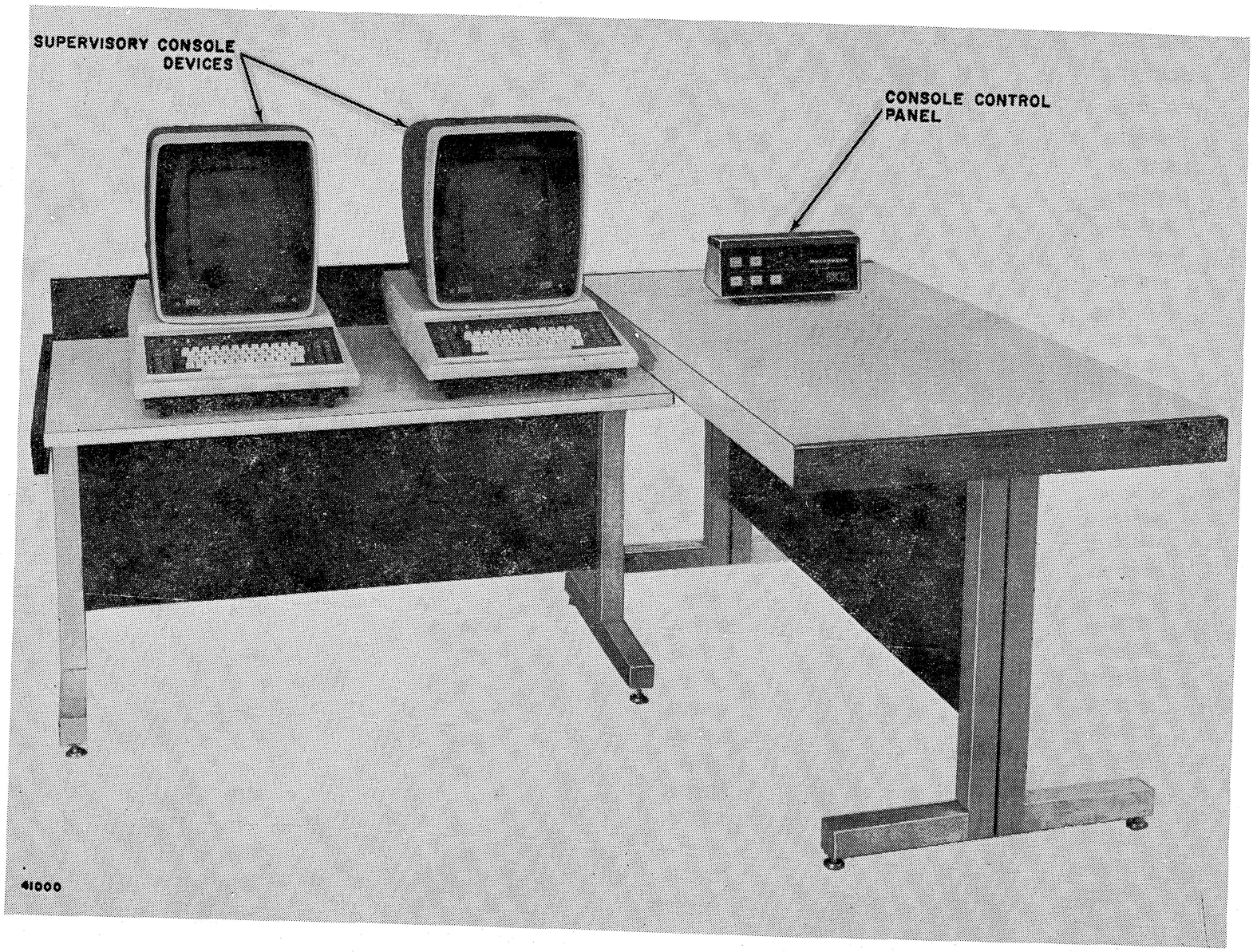


Figure VII-1-1. Operators Control Console

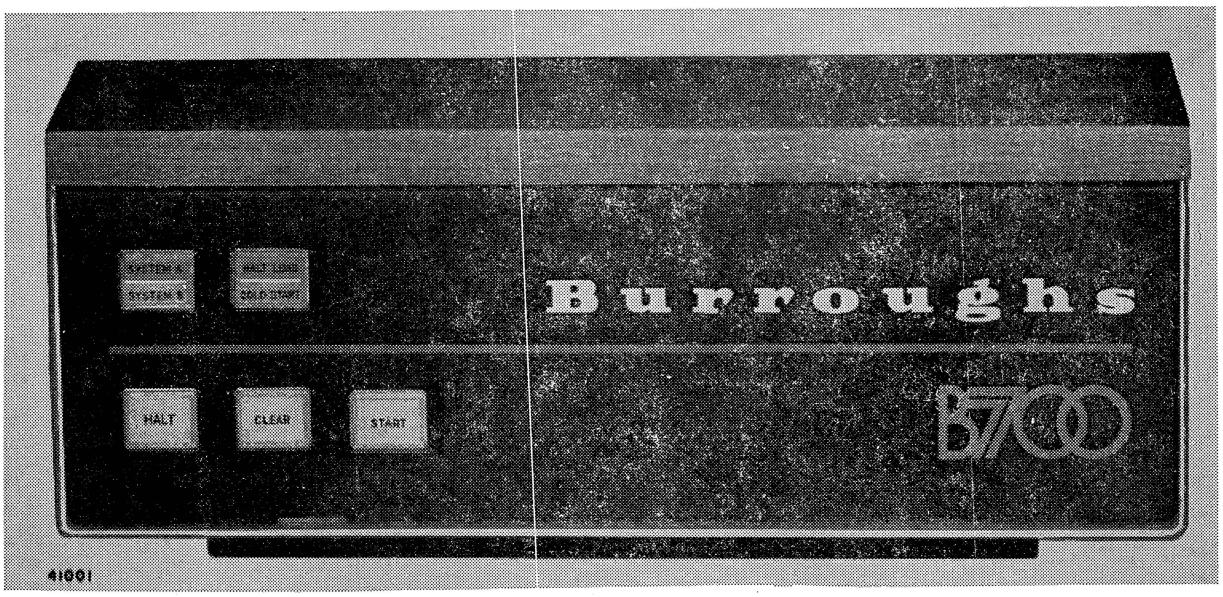


Figure VII-1-2. Console Control Panel

CLEAR - Clears all hard registers and flip-flops to the reset state. Sets IOM's to inhibit state, sets IOM Home Address registers to the memory segment indicated by the switch settings, and clears the peripheral controllers. Sets the MCM requestor inhibit, address limits, and availability registers to the switch settings. Sets the CPM's to control state, control mode 3 in a forced PAUS instruction. Upon receipt of an external interrupt, the CPM will execute code starting at word 8 of the memory segment set into the switch card.

START - Causes the IOM selected as the load IOM to initiate a read operation from either card or disk, depending on the setting of the COLD START/HALT LOAD switch.

If a card load was selected, cards will be read from the card reader specified by the switch settings until a validity check occurs.

If a disk load was selected, 8192 words will be read from address zero of the disk unit specified by the switch settings.

At the completion of the read operation, the CPM specified by the switch settings will be interrupted.

SUPERVISORY CONSOLE

The supervisory console (figure VII-1-3) contains an input keyboard and a video output screen.

KEYBOARD CONTROL KEYS

The following is a list of the keyboard control keys and their functions (Refer to figure VII-1-4).

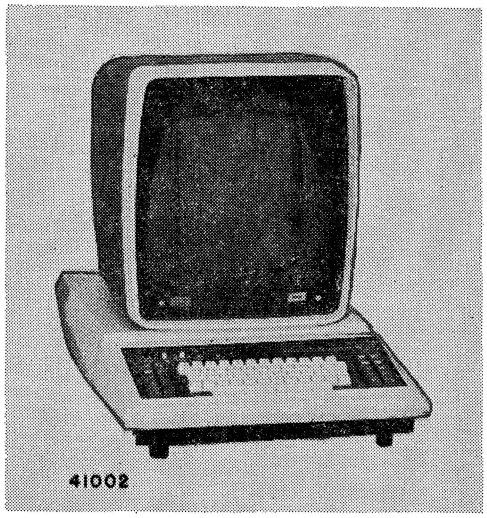


Figure VII-1-3. Supervisory Console

LOC - Places the system in the local mode, which lights the LOCAL indicator.

REC - Places the system in the receive mode, which lights the RECEIVE indicator.

XMIT - Places the system in the transmit mode, which lights the TRANSMIT indicator.

X ETX - End-of-text character. Places the end-of-text character at the cursor location.

↖ HOME - Causes the cursor to be moved to the home (upper left) position.

LINE ERASE - LINE ERASE erases all data in the line except tab flags. Data is erased from the cursor position (including the cursor position) up to and including the last character in the line.

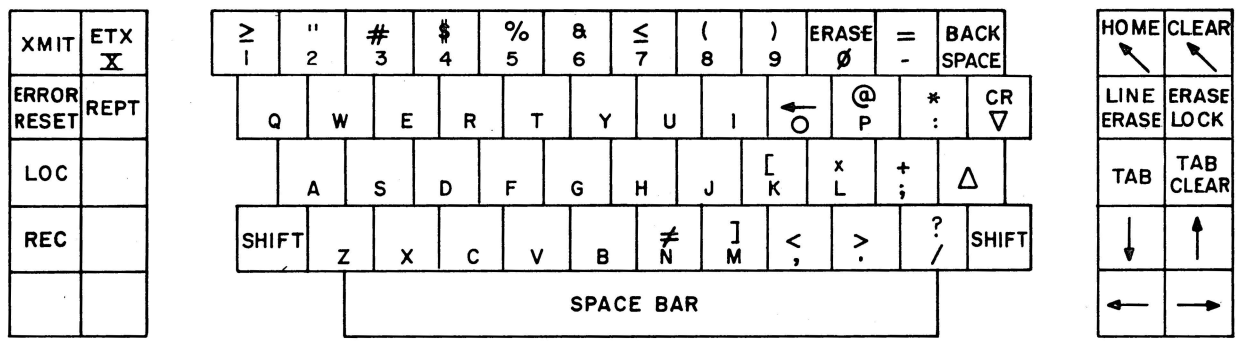
Line Erase will not function unless Erase Lock is depressed simultaneously with Line Erase.

↖ CLEAR - Unshifted - CLEAR erases all data on the screen except tab flags; and, with Forms Option, data bracketed by Shift-In/Shift-Out.

Shifted - CLEAR erases all data on the screen and all tab flags.

CLEAR will not function unless ERASE LOCK is depressed at the same time as CLEAR.

ERASE LOCK - ERASE LOCK is used as an interlock for CLEAR and LINE ERASE. ERASE LOCK must be depressed to permit operation of the CLEAR or LINE ERASE.



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Figure VII-1-4. Keyboard Format

TAB - Unshifted - TAB causes the cursor to move forward to the next tab stop location. If no tab stop is found on a line, the cursor moves to the left edge of the next line.

Shifted - Shifted tab is tab set. Tab set causes a tab stop flag to be entered at the cursor position in all lines.

TAB CLEAR - Unshifted - TAB CLEAR causes the removal of the tab stop flag located at the cursor position in all lines.

↓ (Line Feed) - Line Feed (LF) moves the cursor down one line. When the cursor is in the bottom line, Line Feed causes it to reappear in the top line.

↑ (Reverse Line Feed) - Reverse Line Feed (RLF) moves the cursor up one line. When the cursor is in the top line, RLF causes it to reappear in the bottom line.

← (Backspace) - Backspace (BS) cursor one character. When the cursor is at left edge of page, backspace causes it to reappear at right edge of page in the same line.

→ (Forward Space) - Forward Space (FS) moves the cursor one space to the right. If the cursor is at right edge of page, Forward Space causes it to reappear at the left edge down shifted one line. If the cursor is located in last position of bottom line, Forward Space causes it to reappear in the "home" position.

REPT - If the Repeat key (REPT) is depressed along with any other key except LOC, REC, XMIT, TAB CLEAR, or CLEAR, that other key will be repeated at a rate of about 15 Hertz. When depressed in conjunction with LOC, REC, XMIT, TAB CLEAR or CLEAR Repeat has no effect.

SUPERVISORY CONSOLE OPERATION

The supervisory console unit should be left in REC (receive) mode, except when composing and transmitting input messages to the system. This permits reception of system output messages.

The following steps are necessary to enter an input message.

1. Place the unit in local mode.

2. Position the cursor at the point on the screen where you wish to start typing the message. Normally this is the home (upper left) position; however, messages may be started from any position on the screen.

3. Type in the message.

4. Depress the ETX key. An ETX character will be placed at the current cursor position, and the cursor will move to the home position.

5. If the message was started in other than the home position, position the cursor to the first character of the message.

6. Depress the XMIT key. The transmit indicator will illuminate, and the characters from the current cursor position to the ETX character will be transmitted to the system. Upon completion of the transmission, the unit will return to receive mode.

COLD START/HALT LOAD SELECTION CARD

The COLD START/HALT LOAD Selection Card (figure VII-1-5) mounted in the backplanes of each CPM and IOM contain switches which are used to identify the CPM, MCM, IOM, card reader, and disk file electronics unit to be used when initializing the system.

The COLD START/HALT LOAD Selection Card contains the following switches:

Select (8) - Selects the load IOM. Must be ON for the load IOM, and OFF for all others in that portion of the system.

A/B (7) - Determines which portion of the system (system A or system B) this module belongs to.

MEMORY NO. (1-6) - Indicates the 16K memory segment to be used for initialization (most significant six bits of the memory address). Should be set to 000000.

CPM INTERRUPT NO. (14-16) - Indicates the channel number (binary) of the load CPM, i.e., the CPM which is to be interrupted following the load operation.

CARD READER CHANNEL NO. (9-13) - The number of the channel (internal to the load IOM) to which the load card reader is connected.

DISK FILE CHANNEL NO. (17-21) - The number of the channel (internal to the load IOM) to which the desired disk file exchange is connected.

EU UNIT DESIGNATE NO. (25-32) - The unit designate number of the desired electronics unit. The transfer from the EU will start at SU 0,

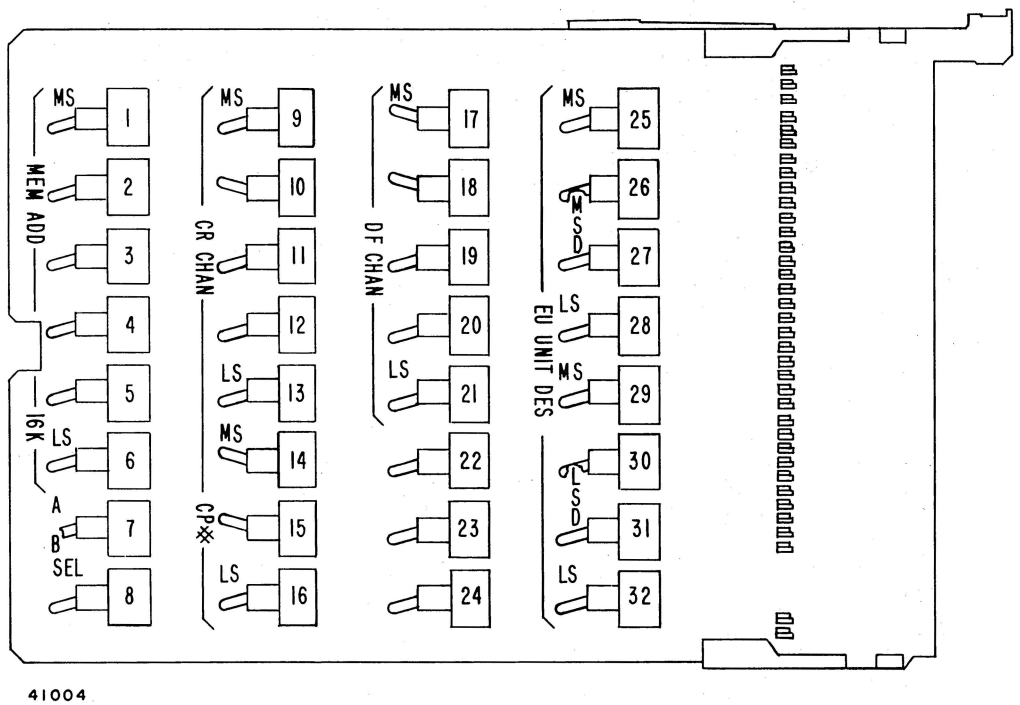


Figure VII-1-5. Cold Start/Halt Load Selection Card

zone 0, track 0, segment 0 of the specified EU.

A CPM uses only the MEMORY NO. and A/B switches. An IOM other than the load IOM uses the SELECT switch (must be OFF), the MEMORY NO., A/B, and CPM INTERRUPT NO. switches. The load IOM uses all switches.

SECTION 2
CENTRAL PROCESSOR MODULE PANELS

This section describes the functions and uses of the controls and indicators on the two panels of the central processor module (CPM). An overall view of the central processor module is shown in figure VII-2-1, and close-ups of the panels are shown in figures VII-2-2 and VII-2-3.

DISPLAY ORGANIZATION

The Central Processor Module has two adjacent panels for display purposes. Each panel has fifteen rows of indicators, a row of 51 toggle switches, and a section of maintenance switches. Legends are printed on the left-hand margin of each panel which indicate the general area a series of rows pertain to. Row numbers are printed on the right-hand margin.

Occasionally, a row of indicators will have two printed row numbers. When this occurs, the single row of indicators is used to display one of two sets of data as specified by a two position toggle switch which is to the left of the row markings. The descriptions of each set either have the format upper switch setting/lower switch setting or are printed above and below the individual indicators.

The indicators within each row are separated into groups of four by color for hexadecimal grouping purposes as is the row of 51 toggle switches.

PANEL 2 INDICATORS (LEFT-HAND PANEL)

EU DATA SECTION

Row 1 - Row 21 Display Selection

The first row of indicators is used to display the contents of either row 1 or row 21. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the first row of indicators and which is labeled EW-C.

Row 1

EU WRITE REGISTER (EW51-0) - The primary input to the Execution Unit (EU) for all data with the exception of operators.

PAR (EW51) - The parity bit of the operand in the EU Write Register (EWR).

TAG (EW50-48) - The tag bits of the operand in the EWR.

Row 21

C REGISTER (C51-0) - The only output from the EU and the input to EU Local Storage. The following EU error checks occur in this register:

1. Some residue generation.
2. All residue checking.
3. All continuity checking.
4. Some parity generation and checking.

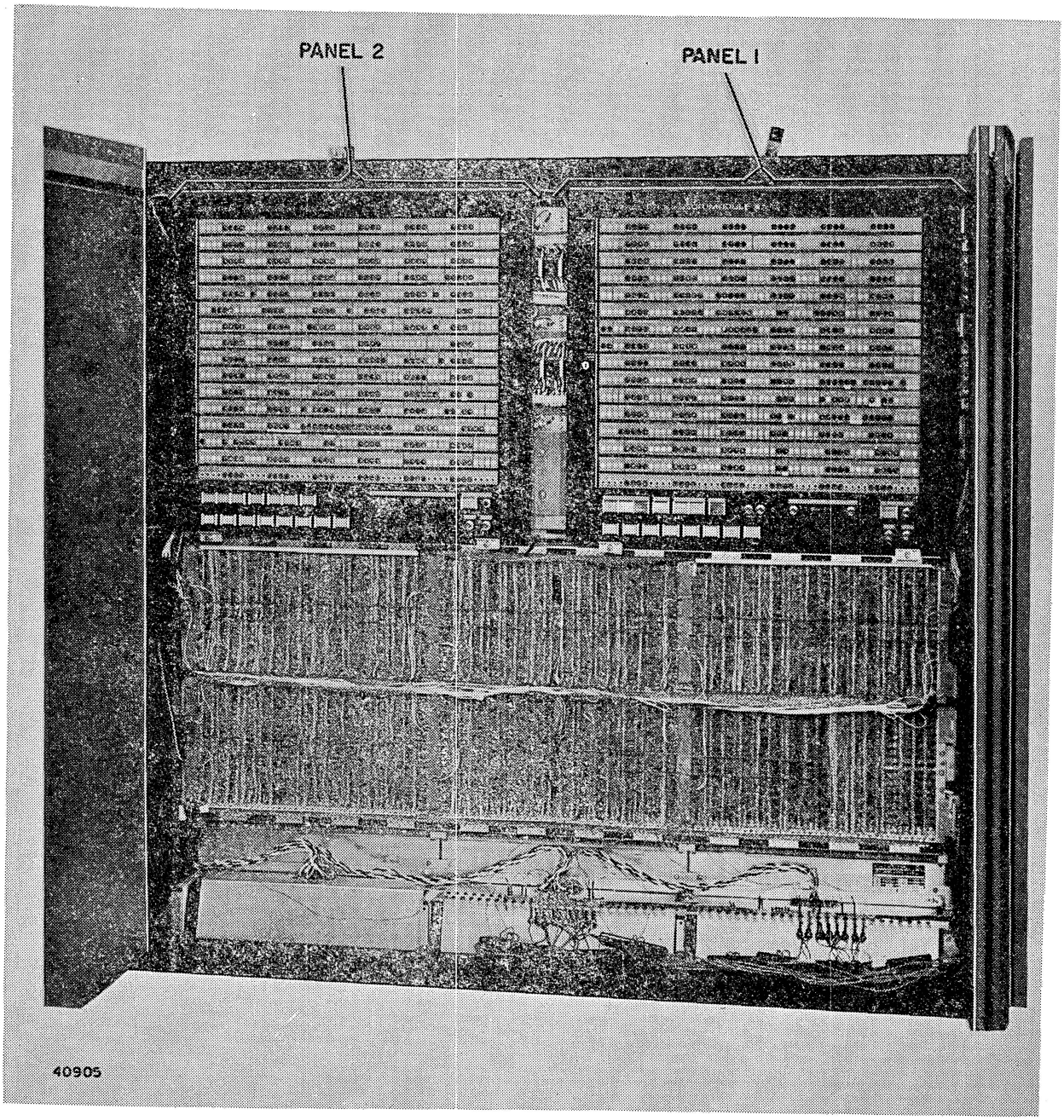
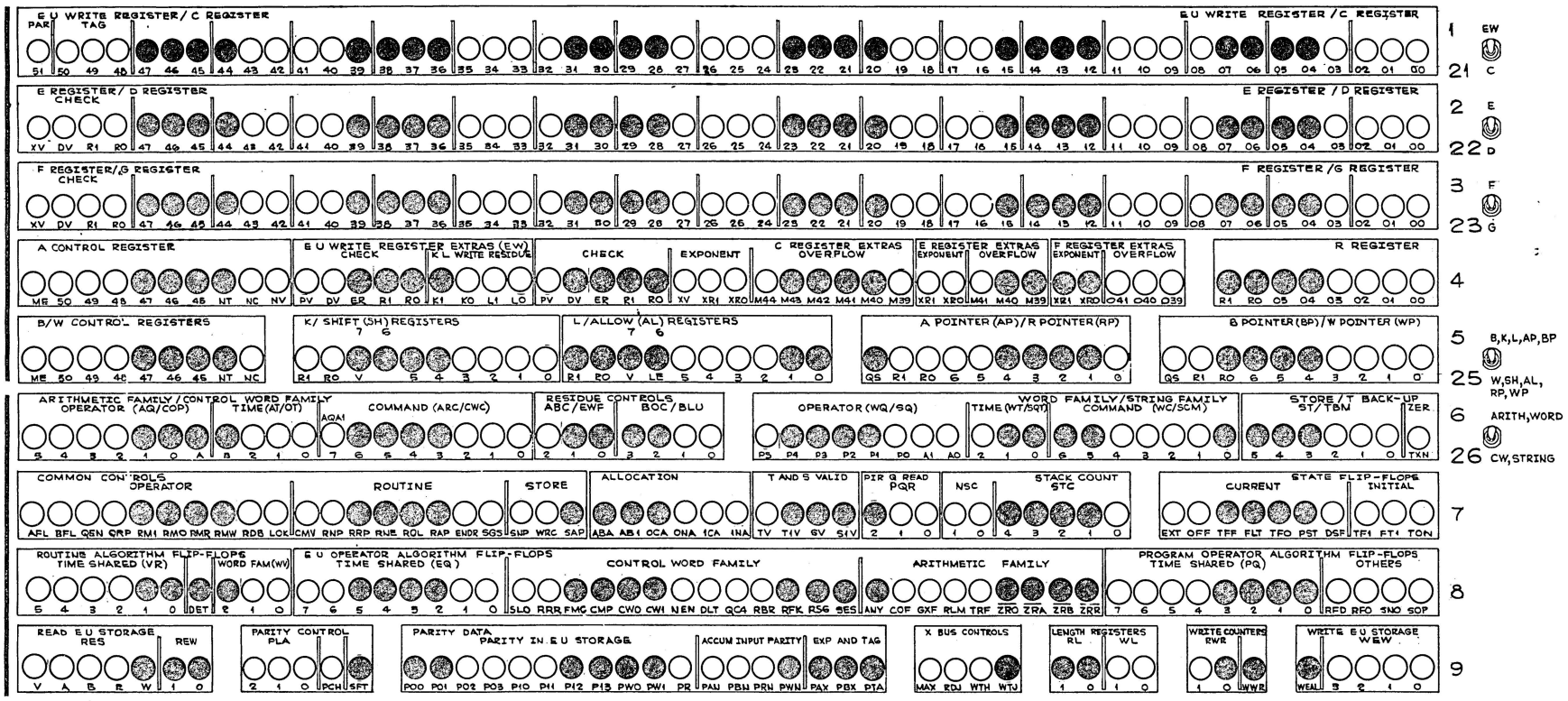


Figure VII-2-1. Central Processor Module

CENTRAL PROCESSOR MODULE



4696A

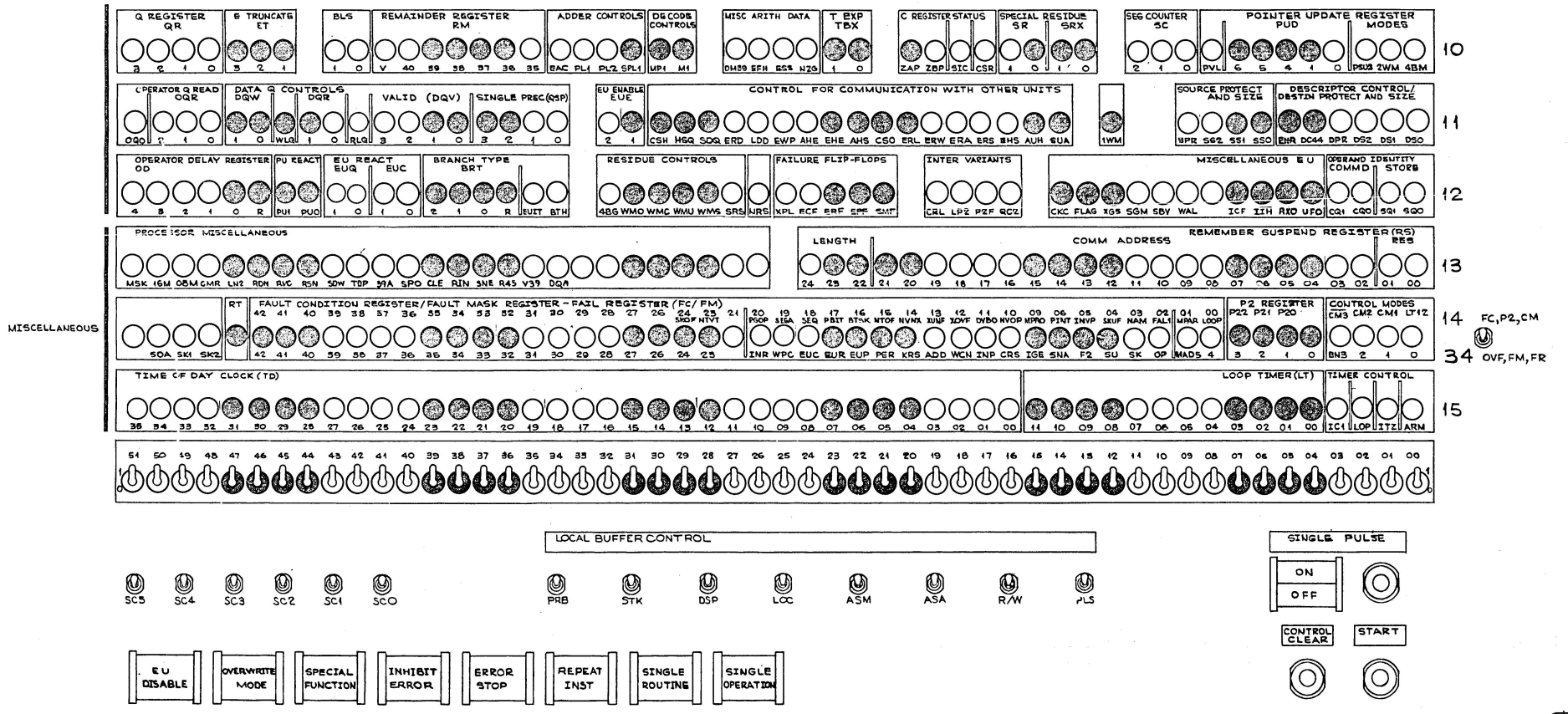
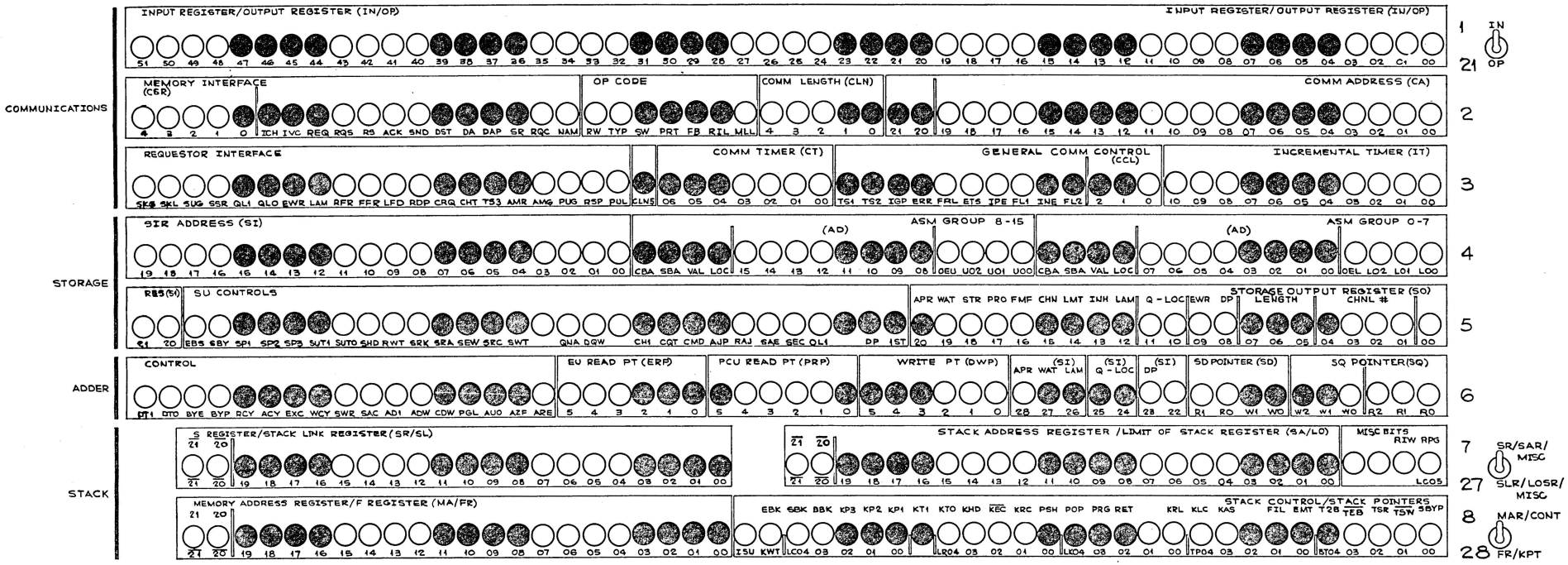


Figure VII-2-2. Panel 2 (Left-Hand Panel) of CPM

CENTRAL PROCESSOR MODULE



409074

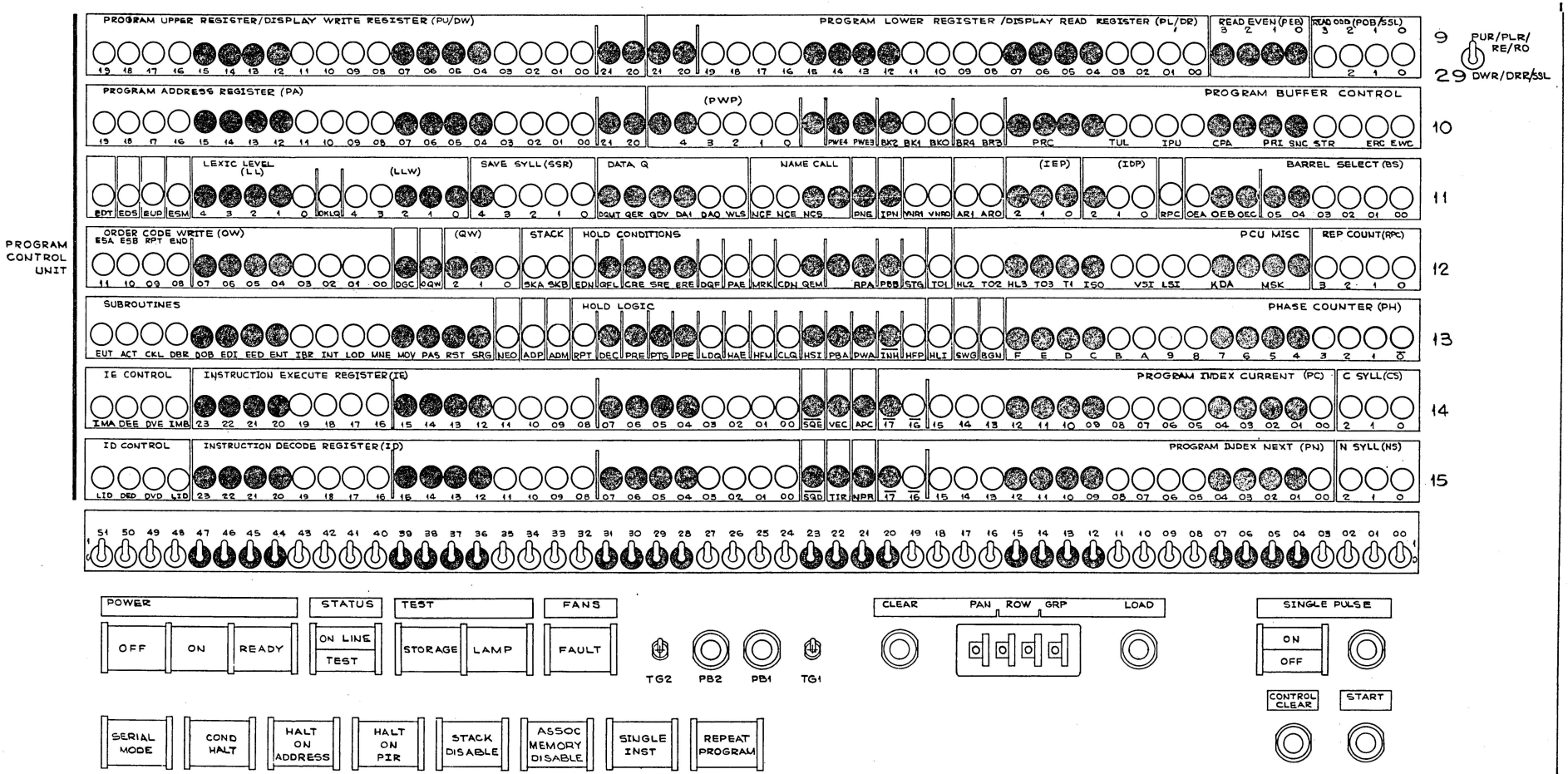


Figure VII-2-3. Panel 1 (Right-Hand Panel) of CPM

PAR (C51) - The parity bit of the operand in the C Register.

TAG (C50-48) - The Tag bits of the operand in the C Register.

Row 2 - Row 22 Display Selection

The second row of indicators is used to display the contents of either row 2 or row 22. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the second row of indicators and which is labeled E-D.

Row 2

E REGISTER

CHECK

XV - EXV is the "E" Register exponent valid bit which is functional in arithmetic mode only.

DV - EDV is the "E" Register data valid bit which indicates validity for either the entire word when in word mode or for the mantissa when in arithmetic mode.

R1,0 - ER1,0 is the "E" Register residue.

BITS 47-0 - E47-0 is the "E" Register which is one of the inputs to the adder and T bus. This register contains the "A" operand when the processor is in Single Instruct.

Row 22

D REGISTER

CHECK

XV - DXV is not used.

DV - DDV is the "D" Register data valid bit.

R1,0 - DR1,0 is the "D" Register residue.

BITS 47-0 - D47-0 is the "D" Register which is the input register to the EU Barrel.

Row 3 - Row 23 Display Selection

The third row of indicators is used to display the contents of either row 3 or row 23. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the third row of indicator and which is labeled F-G.

Row 3

F REGISTER

CHECK

XV - FXV is the "F" Register exponent valid bit which is functional in arithmetic mode only.

DV - FDV is the "F" Register data valid bit which indicates validity for either the entire word when in word mode or for the mantissa when in arithmetic mode.

R1,0 - FR1,0 is the "F" Register residue.

Bits 47-0 - F47-0 is the "F" Register which is one of the inputs to the adder and also feeds the S bus. This register contains the "B" operand when the processor is in Single Instruct

Row 23

G REGISTER

CHECK

XV - GXV is not used.

DV - GDV is the "G" Register data valid bit.

R1,0 - GR1,0 is the "G" Register residue.

Bits 47-0 - G47-0 is the "G" Register which is the third input to the adder.

Row 4

A CONTROL REGISTER - Contains control bits for the "A" operand.

ME - AME indicates an "A" word memory error. The memory control word is returned rather than the expected data.

Bits 50-45 - A50-45 correspond to bits 50-45 in an operand.

NT - ANT indicates that "A" is an integer and is true if bits 45-39 in the "A" operand are zero.

NC - ANC indicates that the "A" operand is in the "C" Register. The contents of "C" thus determine the setting of ANC.

NV - ANV indicates that the "A" Control Register has not yet been completely updated.

EU WRITE REGISTER EXTRAS (EW)

CHECK

PV - EWPV is EWR parity valid

DV - EWDV is EWR data valid

ER - EWER is EWR word parity error. A memory control word has been substituted for the expected data.

R1,0 - EWR1,0 is the EWR residue.

KL WRITE RESIDUE

K1,0 - "K" Register write residue.

L1,0 - "L" Register write residue.

C REGISTER EXTRAS

CHECK

PV - CPV is the "C" Register parity valid bit.

DV - CDV is the "C" Register data valid bit.

ER - CER is the "C" Register memory error bit. A memory control word has been substituted for the expected data.

R1,0 - CR1,0 is the "C" Register residue.

EXPONENT

XV - CXV is the "C" Register exponent valid bit.

XR1,0 - CXR1,0 is the "C" Register exponent residue.

OVERFLOW (M44-39) - CM44-39 are the "C" Register mantissa overflow bits which are an extension for the arithmetics.

E REGISTER EXTRAS

EXPONENT (XR1,0) - EXR1,0 is the "E" Register exponent residue.

OVERFLOW (M41-39) - EM41-39 is the "E" Register mantissa overflow.

F REGISTER EXTRAS

EXPONENT (XF1,0) - FXF1,0 is the "F" Register exponent residue.

OVERFLOW (O41-39) - FO41-39 is the "F" Register mantissa overflow.

R REGISTER

R1,0 - RR1,0 is the "R" Register residue.

Bits 05-0, R05-0 is the "R" Register which is used as both a repeat counter and general accumulator.

Row 5 - Row 25 Display Selection

The fifth row of indicators is used to display the contents of either row 5 or row 25. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the fifth row of indicators and which is labeled B, K, L, AP, BP - W, SH, AL, RP, WP.

Row 5

B CONTROL REGISTER - Contains control bits for the "B" operand.

ME - BME indicates a "B" word memory error. The memory control word is returned rather than the expected data.

Bits 50-45 - B50-45 corresponds to bits 50-45 in an operand.

NT - BNT indicates that "B" is an integer and is true if bits 45-39 in the "B" operand are zero.

NC - BNC indicates that the "B" operand is in the "C" Register. The contents of "C" then determine the setting of BNT.

K REGISTER

R1,0 - KR1,0 is the "K" Register residue.

Bits 7-0 - K7-0 is the "K" Register which is the output of the "K" Queue. The "K" Queue contains the variant for normal operators and the starting bit number within a word for single word string operations.

L REGISTER

R1,0 - LR1,0 is the "L" Register residue.

Bits 7-0 - L7-0 is the "L" Register which is the output of the "L" Queue. The "L" Queue contains the variant for normal operators and the length for string ops on single word operations.

A POINTER (AP) - Used with "A" Local storage and will point at the next character to be used in the "A" operand local storage area.

QS - APQS is the "A" pointer output select.

R1,0 - APR1,0 is the "A" pointer residue.

Bits 6-0 - AP6-0 is the "A" operand shift and allow data to allow the data pointed to to be obtained.

B POINTER (BP) - Used with "B" local storage and will point at the next character to be used in the "B" operand local storage area.

QS - BPQS is the "B" pointer output select.

R1,0 - BPR1,0 is the "B" pointer residue

Bits 6-0 - BP06-0 is the "B" operand shift and allow data pointed to be obtained.

Row 25

W CONTROL REGISTER - General use register.

ME - WME indicates a "W" word memory error. The memory control word is returned rather than the expected data.

Bits 50-45 - W50-45 corresponds to bits 50-45 in an operand.

NT - WNT indicates that "W" is an integer and is true if bits 45-39 in the "W" operand are zero.

NC - WNC indicates that the "W" operand is in the "C" Register. The contents of "C" then determine the setting of WNT.

SHIFT REGISTER (SH) - Shift factors for the EU Barrel in octades and bits.

R1,0 - SHR1,0 is the Shift Register residue.

V - SHV is shift valid

Bits 5-0 - SH5-0 is the Shift Register.

ALLOW REGISTER (AL) - Allows "n" bits out of the EU Barrel.

R1,0 - ALR1,0 is the Allow Register residue.

V - ALV is Allow Register valid.

LE - ALLE is allow left.

Bits 5-0 - AL05-0 is the Allow Register.

R POINTER (RP) - Used with "R" Local storage which holds the local destination information for string ops and is used for miscellaneous arithmetic partial results.

QS RPQS is the "R" pointer output select.

R1,0 - RPR1,0 is the "R" pointer residue.

Bits 6-0 - RP06-0 is the "R" storage shift and allow data to allow the indicated character to be obtained.

W POINTER (WP) - Used with "W" local storage which holds the local source information for string ops and is used for miscellaneous arithmetic functions.

QS - WPQS is the "W" pointer output select.

R1,0 - WPR1,0 is the "W" pointer residue

Bits 6-0 - WP06-0 is the "W" storage shift and allow data to allow the indicated character to be obtained.

EU CONTROL SECTION

Row 6 - Row 26 Display Selection

The sixth row of indicators is used to display the contents of either row 6 or row 26. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the sixth row of indicators and which is labeled ARITH, WORD-CW, STRING.

Row 6

ARITHMETIC FAMILY

OPERATOR (AQ)

Bits 5-0 - AQ5-0 is the Arithmetic Family Operator Register which contains the internal micro-op from either the EU Operator Queue, or if that is empty, directly from the OW Register. The contents of the Operator Register will cause the generation of certain commands or routines to be done to complete a required task.

A - AQA is the allow bit for the Arithmetic Family. The Operator Registers of all families are loaded simultaneously, the allow bit indicates when its associated operator register is active.

TIME (AT3-0) - The Arithmetic Family operator Timer.

COMMAND (ARC)

AQA1 - Duplicate of AQA for loading purposes.

Bits 6-0 - ARC6-0 is the Arithmetic Family Command Register which contains the code of a command to perform a simple function (e.g., load a register).

RESIDUE CONTROLS

ABC2-0 - A type of command register for the Adder and Barrel for residue correction.

BOC3-0 - Barrel Residue correction

WORD FAMILY

OPERATOR (WQ)

P5-0 - WQP5-0 is the Word Family Operator Register which contains the internal micro-op from either the EU Operator Queue, or if that is empty, directly from the OW Register. The contents of the Operator Register will cause the generation of a certain command or routine.

A1,0 - WQA1,0 is the allow bit for the Word Family. The Operator Registers of all families are loaded simultaneously. The allow bit indicates when its associated operator register is active.

TIME (WT2-0) - The Word Family operator Timer.

COMMAND (WC6-0) - The Word Family Command Register which contains the code of a command.

STORE

Bits 5-0 - ST5-0 is the Store Command Register. It contains source and destination codes to enable data and address transfers outside of the EU.

ZER - The "R" Register is zero.

Row 26

CONTROL WORD FAMILY

OPERATOR (COP)

Bits 5-0 - COP5-0 is the Control Word Family Operator Register which contains the internal micro-op from either the EU Operator Queue, or if that is empty, directly from the OW Register. The contents of the Operator Register will cause the generation of a certain command or routine.

A - COPA is the Allow bit for the Control Word Family. The Operator Registers of all families are loaded simultaneously. The allow bit indicates when its associated operator register is active.

TIME (OT3-0) - The Control Word Family operator Timer.

COMMAND (CWC7-0) - The Control Word Family Command Register which contains the code of a command.

RESIDUE CONTROLS

EWF2-0 - E, EWR, or F residue combined with Barrel residue. A code for the Specific type of combination.

BLUE2-0 Barrel or Logic Unit Residue Correction.

STRING FAMILY

OPERATOR (SQ)

P5-0 - SQP5-0 is the String Family Operator Register which contains the internal micro-op from either the EU operator Queue, or if that is empty, directly from the OW Register. The contents of the Operator Register will cause the generation of commands or routines.

A1,0 - SQA1,0 are the Allow bits for the String Family. The Operator Registers of all families are loaded simultaneously. The allow bit indicates when its associated operator is active.

TIME (SQT2-0) - The string Family operator timer.

COMMAND (SCM6-0) The String Family Command Register which contains the code of a command.

T BACK-UP

TBM - TBM5-0 is the T Back Up which is a coded source for additional data for the T Buss.

TXN - T Back-up Register is not valid for an exponent.

Row 7

COMMON CONTROLS

OPERATOR

AFL - "A" full (at the start of the current EU operator).

BFL - "B" full (at the start of the current EU operator).

QEN - Last EU operator of any sequence sent by the PCU.

QRP - Send report back to the PCU on the last command of the current operation (when the report bit is set).

RM1-0 - Remember the current operator family and indicates which family is doing the operation.

RMR - Remember return to the Control Word Family. This is used to return when a micro-op calls a micro-op of a different family.

RMW - Remember return to the Word Family. This is used to return when a micro-op of a different family.

RDB - Do a REDB (read "B") operator at the completion of the current operator.

LOK - Lock K and L.

ROUTINE

CMV - Command variant to remember extra operand.

RNP - Routine end of program operator (follows QEN).

RRP - Routine send report (follows QRP)

RNE - Routine end of EU operator. This indicates the final routine of a micro-op.

ROL - Routine operator load which indicates that the EU has generated a micro-op. The operator registers are loaded as a result of the command register contents.

RAP - Routine advance of the PIR Queue read pointer.

ENDR - End of routine.

SGS - Single routine STOP which reflects the status of the Single Routine Stop button.

STORE

SNP - Store Level end of program operator. The result is in the C Register. This flip-flop is set after RNP is set.

WRC - Read allocation change. There has been a change in the allocation flip-flops.

SAP - Store Level, advance. PIR Queue read pointer (from setting of RAP).

ALLOCATION

ABA - The current A/B allocation in EU local storage.

AB1 - The initial A/B allocation in EU local storage.

OCA - The current read allocation for the first group of EU local storage.

ONA - The initial read allocation for the first group of EU local storage.

1CA - The current read allocation for the second group of EU local storage.

1NA - The initial read allocation for the second group of EU local storage.

T AND S VALID

TV - The T Buss was valid during the previous time.

T1V - T initial valid. The T Buss will be valid at the end of the program operator.

SV - The S Buss was valid during the previous time.

S1V - S initial valid. The S Buss will be valid at the end of the program operator.

PIR Q READ (PQR2-0) - The PIR Queue read pointer. The PIR Queue associates a program operator PIR address with a micro operator for interrupt purposes.

STACK COUNT

NSC - NSC2-0 is the New Stack Count and is used to count the pushes or pops done by a program operator. The NSC is added to STC to arrive at a new stack arrangement at the completion of the program operator.

STC - STC4-0 is the Stack Count which is used to re-establish the stack after an interrupt.

STATE FLIP-FLOPS

CURRENT

EXT - Mantissa sign of the "A" operand.

OFF - Overflow

TFF - True/false flip-flop

FLT - Float mode-used in edit operations.

TFO - True/false flip-flop occupied (valid).

PST - Processor state-normal mode.

DSF - Different segment

INITIAL

TF1 - True/false initial, the initial setting of TFF.

FT1 - Float mode initial

TON - True/false occupied initial.

Row 8

ROUTINE ALGORITHM FLIP-FLOPS

TIME SHARED (VR) - VR5-0 contain the EU routine variants.

DET - Descriptor size transfer.

WORD FAM (WV) - WV2-0 contain the Word Family variants.

EU OPERATOR ALGORITHM FLIP-FLOPS

TIME SHARED (EQ) - EQ7-0 contain the EU program operator variants

CONTROL WORD FAMILY

SLO - The store level for the last operator from the EU Operator Queue.

RRR - Remember to return at the end of a routine rather than exiting. This is used when one routine has called another routine.

FMC - Family "C" operator (first hex digit is "A").

CMP - Compare

CWO,1 - Control word remember controls.

NEN - No End (of program op.)

DLT - Delete T

QC4 - Remember SIRW

RBR - Remember dynamic branch

RFK - Remember to fetch stack

RSG - Remember segmented description.

SES - Load associative memory.

ARITHMETIC FAMILY

ANY - Any 1 in truncated segment. Is there a 1 in E Truncate which is an extension of the "E" Register for arithmetic purposes.

COF - Carry out

GXF - Greater exponent

RLM - Right to left mode

TRF - Truncate

ZRO - Remember zero

ZRA - The "A" operand is zero

ZRB - The "B" operand is zero

ZRR - The result is zero

PROGRAM OPERATOR ALGORITHM FLIP-FLOPS

TIME-SHARED (PQ) - PQ7-0 contain the program operator variants.

OTHERS

RFD - Remember flashback for data

RFO - Remember flashback occurred.

SNO - Special action if integer overflow.

SOP - Source is an operand.

Row 9

READ EU STORAGE

RES

V - RESV is EU read valid

A - RESA is read within first 4 words of EU storage

B - RESB is read within second 4 words of EU storage

R - RESR is read within third 4 words of EU storage

W - RESW is read within fourth 4 words of EU storage

REW - REW1,0 contains the EU read address within four word groups.

PARITY CONTROL

PLA - PLA2-0 is parity look ahead, a code indicating what type of parity to check.

PCH - Parity check

STF - Store first time

PARITY DATA

PARITY IN EU STORAGE

POO-13 - Parity bits for EU local storage in A and B areas.

PWO,1 - Time shared "W" Register parity.

PR - Time shared "R" Register parity

ACCUM INPUT PARITY

PAN - Accumulate indicated parity for "A"

PBN - Accumulate indicated parity for "B"

PRN - Accumulate indicated parity for "R"

PWN - Accumulate indicated parity for "W"

EXP AND TAG

PAX - "A" operand exponent indicated parity

PBX - "B" operand exponent indicated parity

PTA - Tag indicated parity.

BUS CONTROLS

MAX - Main adder Transfer to the X Buss.

RDJ - Read to "J" storage (auxiliary storage location). When reset, read to "H" storage.

WTH - Write to "H" storage (auxiliary storage location)

WTJ - Write to "J" storage (auxiliary storage location)

LENGTH REGISTERS

RL - RL1,0 contains the "R" storage length in EU Local storage (in number of words)

WL - WL1,0 contains the "W" storage length in EU Local storage (in number of words)

WRITE COUNTERS

RWR - RW1,0 contains the "R" storage write counter.

WWR - The "W" storage write counter

WRITE EU STORAGE

WEAL - Write allow for EU local storage

WEW - WEW3-0 contains the write address for EU local storage

Row 10

Q REGISTER (QR30-0) - The Trial Quotent Register used in division.

E TRUNCATE (ET3-1) - The "E" Register Truncate bits.

BLS (BLS1,0) - Contain the binary shift left factor for division

REMAINDER REGISTER (RM)

V - RMV is remainder register invalid.

Bits 40-35 - RM40-35 is the remainder register

ADDER CONTROLS

EAC - End around carry

PL1 - Plus 1

PL2 - Plus 2

SPL1 - Special plus 1, used when a "double carry" occurs

DECODE CONTROLS

MP1 - Multiplier plus 1

M1 - Mode 1 for the scale right operator.

MISC ARITH DATA

DM39 - The "D" Register mantissa bit 39 which indicates overflow from the mantissa into the exponent.

EFH - "E" and "F" Registers exponent hold which causes the valid bit of the "E" and "F" exponent register's not to be reset.

If this command was not issued, the data valid bit would normally be automatically reset in the next clock eventually resulting in a continuity error.

ESS - EU Local storage Transfer to the "S" Buss (The normal Transfer is to the "T" Buss).

NZG - Zeros were not loaded to the "G" Register.

TEXP (TBX1,0) - The "T" Buss back up exponent used for exponent overflow during arithmetic operations.

C REGISTER STATUS

ZAP - The number of leading zeros in the "C" Register have been counted, and the result has been placed in the "A" pointer.

ZBP - The number of leading zeros in the "C" Register have been counted, and the result has been placed in the "B" pointer.

SIC - The contents of the "S" Buss have been transferred to the "C" Register. (The normal transfer is from the "T" Buss to the "C" Register).

CSR - "C" Register residue has been placed in Special Residue. This action saves regenerating the residue when the contents of the "C" Register are placed in EU local storage for a short period of time. EU local storage has no capacity for the storage of residue.

SPECIAL RESIDUE.

SR - SR1,0 is the special residue for the "C" Register mantissa (see CSR).

SRX - SRX1,0 is the special residue for the "C" Register exponent (see CSR).

SEG COUNTER (SC2-0) - A segment counter used to keep track of words, used in conjunction with the pointers.

POINTER UPDATE REGISTERS

PVL - Pointer update register valid

PUD - PUD6-4 is a word update for the EU local storage pointers.

PUD3-0 is a digit update for the EU local storage pointers.

MODES

PSUB-Subtract pointer update register.

2WM - Two word mode for EU local storage pointers.

4BM - Four bit mode for EU local storage pointers (normally information is dealt with in three bit digits).

Row 11

OPERATOR Q READ

OQO - Operator queue occupied.

OQR - OQRZ-0 is the operator queue read register.

DATA Q CONTROLS

DQW - DQW1,0 is the data queue write register.

WLQ - Write into the least significant word of the double precision data queue entry.

DQR - DQR1,0 is the data queue read register.

RLQ - Read from the least significant word of the double precision data queue entry.

VALID (DQV3-0). The data queue valid register which is used to allow a inhibit reads and writes. Each double precision data queue entry is represented by a bit in DQV. The bit must be true to enable a read and false to enable a write.

SINGLE PREC (QSP3-0) - Used to indicate single precision operand in each of the data queue entries.

DQA - Data queue read pointer advance.

EU ENABLE (EUE2-1) - Enables the clock for the EU.

CONTROL FOR COMMUNICATION WITH OTHER UNITS

CSH - Conditional stack hold. Enables hold for stack buffer if necessary.

HSQ - Hold for Storage unit data queue available.

SDQ - Store to storage unit data queue.

ERD - EU request for address unit read.

LDD - EU request for address unit quick write.

EWP - Enable address unit write pointer.

AHE - Address unit hold and conditional EU hold for EWR.

EHE - EU hold for EWR data valid.

AHS - Address unit transfers to MAR.

CSO - "C" Register transfer to MAR.

ERL - Conditional request for EWR.

ERW - Unconditional request for EWR.

ERA - Address unit controlled by EU.

ERS - EU request for storage unit.

EHS - EU hold for storage unit available.

AUH - Address Unit hold.

SUA - Storage Unit abort.

1WM - One word mode for string operators.

SOURCE PROTECT AND SIZE

SPR - Source memory protect

SS2-0 - The source size register which contains the character size.

DESCRIPTOR CONTROL/DESTIN. PROTECT AND SIZE

DC44 - "D" Control Register bit 44 which indicates that data is segmented.

DPR - Destination protect

DS2-0 - Destination Size Register which contains the character size.

Row 12

OPERATOR DELAY REGISTER (OD)

Bits 4-0 - OD4-0 contain the Operator Delay Register which holds the code for an interrupt while the existing command is finished. The delay is for one clock.

R - ODR is the operator delay restore bit which enables restart of a program operator after an interrupt. If ODR is true, then A/B Initial will be left as is, however, if ODR is false then A/B Initial is moved to A/B Current.

PU REACT (PU1,0) - The equivalent of an interrupt caused by a series of micro-ops. This mechanism allows variation of a micro-op.

EU REACT

EUQ - EUQ1,0 is the EU operator react which is the equivalent of an interrupt caused by a series of micro-ops. This mechanism allows variation of a micro-op.

EUC - EUC1,0 is the EU command react which is similar to EUQ except it allows variation of routines.

BRANCH TYPE

BRT

BITS 2-0 - BRT2-0 contain the branch (interrupt) type.

R - BRTR is branch type restore.

EUIT - EU in Trouble. This mechanism is used for synchronization between the EU and PCU and is evoked when a change in direction occurs and it becomes necessary to call a hardware subroutine.

BTH - Branch type hold which holds the EU while the EU operator queue is invalidated.

RESIDUE CONTROLS

4BG - Four bit residue generator mode for string operators only.

WMO - The word residue mode command which indicates the type of residue.

WMC - Word residue mode is conditional as "S" Register validity.

WMU - Word residue mode unconditional

WMS - Word residue check mode.

SRS - Suppress residue check on sign.

NRS - No restart. If set on STOP ON ERROR, the micro-op cannot be repeated.

FAILURE FLIP-FLOPS.

XPL - Extra pointer load which indicates that an attempt was made to load a pointer while the existing contents were valid. The existing pointer information was thus not shifted somewhere else before the attempted move, or an incorrect hold data valid was issued. or an incorrect hold data valid was issued.

ECF - EU continuity failure

ERF - EU residue failure

EPF - EU parity failure

SMF - String memory failure

INTER VARIANTS

CRL - Created Length

LP2 - PCU load P2 if interrupt

P2F - P2 contains data

QC2 - Inhibit normal interrupt

MISCELLANEOUS EU

CKC - Chech "C" Register continuity.

FLAG - Remember illegal shift, start, or length.

XGS - Exponent difference greater than selected leading zeros which indicates that the exponent was too large to use only the exponent shift.

SGM - Single routine mode.

SBV - Stack Buffer valid.

WAL - "W" Register allocation.

ICF - Interrupt channel "n"

IIH - Inhibit external interrupts (DEXI)

RXO - Remember exponent overflow.

UFO - Underflow zero micro-op next.

OPERAND IDENTITY

COMMD (CQ1,0) is the command operand which acts as a variant on the command.

STORE (SQ1,0) is the "check" operand which acts as a variant on the store.

MISCELLANEOUS SECTION

Row 13

PROCESSOR MISCELLANEOUS

MSK - Master synchronization flag to keep 8 and 16 megahertz cooperative.

16M - Sixteen megahertz clock

08M - Eight megahertz clock

CMR - Command register zero check

LN2 - Fetch length equals 2

RDN - Remember different stack number

RVC - Remember value call

RSN - Restart next operator

SDW - Store to "D" Register word

TDP - Take double precision

39A - 39 bit adder mode

SPO - String program operator

CLE - Clear EU controls

RIN - Repeat instruction

SNE - Store level end of EU operator

R45 - Set bit 45 in P1 if RETN presence bit

V39 - Set bit 39 in P1 if VALC presence bit

DQA - Data queue available

REMEMBER SUSPEND REGISTER (RS) - Holds the control word if a multiword fetch by the PCU for the program buffer is interrupted. The PCU has the lowest priority with the COMM. Unit.

LENGTH (RS24-22) - The number of words remaining to be read.

Comm Address - (RS21-2) - The main memory address.

RES (RS01,0) - Comm address residue.

Row 14 - Row 34 Display Selection

The fourteenth row of indicators is used to display the contents of either row 14 a row 34. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the fourteenth row of indicators and which is labeled FC, P2, CM - OVF, FM, FR.

Row 14

SOA, SK1, SK2 - Special stack control for interrupts.

RT - Return for interrupt. This is equivalent to bit 46 of the fault condition register and indicates that a return rather than an exit should be done after interrupt processing.

FAULT CONDITION REGISTER

SKOF - Stack overflow

NTVT - Interval timer

PGOP - Programmed operator

SEGA - Segmented array

SEQ - Sequence error

PBIT - Presense bit

BTSK - Bottom of stack

NTOF - Integer overflow

NVNX - Invalid index

XUNF - Exponent underflow

XOUF - Exponent overflow

DVBO - Divide by zero

NVOP - Invalid operand

NPRO - Memory protect

PINT - Processor internal

INVP - Invalid program word

SKUN - Stack underflow

NAM - Invalid address (no access to memory)

FAL1 - Memory fail 1 (2 or more bits in error)

NPAR - Memory parity

LOOP - Loop

P2 REGISTER (P22-20) - P2 parameter register for interrupts.

CONTROL MODES (CM3-0) - Interrupt management level of the processor.

Row 34

SOA, SK1, SK2 - Special stack control for interrupts.

FAULT MASK REGISTER - FAIL REGISTER (FM)

BITS 42-23 - FM42-23 is the Fault Mask Register which enables or disables recognition of the special (third priority) and external (fourth priority) interrupts.

INR - Inhibit normal return

WPC - Counter residue

EUC - EU continuity

EUR - EU residue

EUP - EU parity

PER - Program Unit error

KDS - Stack residue

ADD - Adder unit residue

WCN - Wrong channel number

INP - Parity to the Comm. Unit

CRS - Comm. Unit residue

IGE - Ignore error

SNA - Special no access

F2 - One bit error

SU - Storage Unit

SK - Stack

OP - Operation

MADS5-0 - Memory address for interrupts

BN3-0 - Box number for interrupts.

Row 15

TIME OF DAY CLOCK (TD35-0) - The time of day in 2 microsecond intervals.

LOOP TIMER (LT11-0) - A two second timer in the processor that is retriggered with the completion of each program operator based in Final Command Final Routine.

TIMER CONTROL

IC1 - Loop timer overflow control

LOP - LOOP timer overflow

ITZ - Incremental timer zero

ARM - Incremental timer overflow

PANEL 2 SWITCHES (LEFT-HAND PANEL)

SC5-0 - Not wired

LOCAL BUFFER CONTROL

PRB - Used in manually reading and writing the program buffer.

STK - Used in manually reading and writing the stack buffer.

DSP - Used in manually reading and writing The Display Buffer.

LOC - Used in manually reading and writing EU Local Storage

ASM - Used in manually reading and writing Associative Memory - data.

ASA - Used in manually reading and writing Associative Memory addresses, together with ASA.

R/W - Used in conjunction with the other Local buffer controls to designate a Read (false) or Write (true) operation.

PLS - A momentary contact switch used for pulsing in conjunction with the other local buffer controls to actually transfer in or out of the local storage.

SINGLE PULSE

ON-OFF - This indicator/switch enables or disables the Single Pulse junction. If this switch is on, the Special Function switch must also be on.

Push Button - Used for single pulsing. When this switch is depressed, one eight-megacycle and two sixteen-megacycle clocks are generated.

EU DISABLE - Disables communication with the EU. This is used for working with the PCU a Storage Unit without interference from the EU.

OVERITE MODE - Changes all stores to overwrites

SPECIAL FUNCTION - Syncs clocks on Single Pulse operation.

INHIBIT CLEAR - Keeps execution errors from stopping unit.

ERROR STOP - Stops unit on internal hardware errors. If an internal interrupt occurs, bit 6 row 14 will be set.

REPEAT INST - Causes loop on instruction that caused unit to stop on error STOPj Must be pressed after unit has stopped on error.

SINGLE ROUTINE - Causes execution of a single routine within an instruction. (Execution of single EU operator).

CONTROL CLEAR - General processor clear.

START - Starts processor. This switch is also used to continue from some types of halt conditions.

PANEL 1 INDICATORS (RIGHT HAND PANEL)

COMMUNICATIONS SECTION

Row 1 - Row 21 Display Selection

The first row of indicators is used to display the contents of either row 1 or row 21. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the first row of indicators and which is labeled IN-OP.

Row 1

INPUT REGISTER (IN51-0) - The input register to the Comm Unit which is used for data transfer between the processor and memory.

Row 21

OUTPUT REGISTER (OT51-0) - The output register from the Comm. Unit which is used for data transfer between memory and the processor.

Row 2

MEMORY INTERFACE

CSR - CSR4-0 is the Comm. Select Register which contains the number of the physical MCM selected.

ICH - Inhibit Comm. halt.

IVC - Invalid channel

REQ - Request

RQS - Request strobe

RS - Request special

ACK - Acknowledge

SND - Send data

DST - Data strobe

DA - Data available

DAP - Data present

S/R - Send/receive. A value of false indicates Send, True indicates Receive.

RQC - Requestor operation complete.

NAM - No access to memory.

OP CODE - Operator and control bits for the memory control word.

RW - Read/Write. A value of false indicates Read, True indicates a Write.

TYP - Type

SW - Single word

PRT - Protect

FB - Flashback

RIL - Requestor inhibit load

MLL - Memory Limit Load

COMM LENGTH - CLN5 (ROW 3 BIT 31) and CLN4-0 contain the length of the operation in words.

COMM ADDRESS (CA19-0) The absolute memory address.

Row 3

REQUESTOR INTERFACE - Internal processor requestors to the Comm Unit.

SKG - Stack operation granted

SKL - Stack last word

SUG - Storage Unit operation granted

SSR - Sync Storage Unit request

QL1,0 - EU Data Queue location

EWR - Write into the EU Write Register

LAM - Load Associative Memory

RFR - Request processor fail register fetch fetch

FFR - Fetch processor fail register.

LFD - Look for double precision

RDP - Remember double precision which indicates that the second word of a double precision number is being "fetched"

CRQ - Comm requests SU Data Queue

CHT - Comm hlt

TRG - EWR data transfer request granted.

AMR - Comm. requests Associative Memory

AMG - Comm. Associative Memory request granted.

PUG - Program Unit operation granted

RSP - Remember Program Unit operation suspended.

PUL - Program Unit last word

CLN5 - The most significant of the Comm Length (CL) Located in row 2 bits 26-22.

COMM TIMER (CT6-0). Timer for Comm. Unit operations.

GENERAL COMM CONTROL

TS1 - Transfer sync 1

TS2 - Transfer sync 2

IGP - Ignore data parity

ERR - Comm error

FRL - Processor fail register locked

ETS - Error Transfer sync

IPE - Internal parity error

FL1 - Memory fail 1 (2 or more bit error)

INE - Internal error

FL2 - Memory fail 2 (1 bit error)

CCL - CCL2-0 is the Comm. cancel length.

INCREMENTAL TIMER (IT10-0) - The interval timer.

STORAGE SECTION

Row 4

SIR ADDRESS (SI19-0) - The Storage Input Register Address which is an absolute memory address. This register inputs to the SU operator queue.

ASM GROUP 8-15 - Associative Memory information.

CBA - Comm. busy with Associative Memory

SBA - Storage Unit busy with Associative Memory

VAL - Valid. The Local (LOC) is valid.

LOC - Local. The MAR address compares to an ASM address.

AD - AD15-8 contains Associative Memory addressing for local checks. When set, indicates that a comparison has been found and enables the read.

OEU - Oldest entry upper.

U02-00 - Upper pointers for loading information into Associative Memory.

ASM GROUP 0-7 - Associative Memory information.

CBA - Comm. busy with Associative Memory

SBA - Storage Unit busy with Associative Memory

VAL - Balid. The Local (LOC) is valid.

LOC - Local. The MAR address compares to an ASM address.

AD - AD7-0 is Associative Memory addressing for Local checks.

OEL - Oldest entry lower.

LO2-0 - Lower pointers for loading.

Row 5

RES - Residue for The Storage Input Register

SU CONTROLS

EBS - Execution Unit busy with The Storage Unit.

SBY - Storage Unit busy.

SP1 - Storage Unit phase 1

SP2 - Storage Unit phase 2

SP3 - Storage Unit phase 3

SUT1 - Storage Unit time 1

SUT0 - Storage Unit time 0

SHD - Storage Unit Hold (disable time 0).

RWT - Remember wait

SRK - Storage Unit requests stack

SRA - Storage Unit requests Associative Memory

SEW - Storage Unit requests EWP

SEC - Storage Unit end of cycle

SWT - Storage Unit write

RSD - Not Used.

QNA - Storage Unit Data Queue not available

DQW - Storage Unit Data Queue write

CHI - Request Comm. halt

CQT - Request Comm. quit

CMD - Comm. done

AJP - Adjust Storage Unit Data Queue read pointer

RAJ - Remember Storage Unit Data Queue read pointer adjusted

SAE - Storage Unit address to EWR

OL1 - Original length one word

DP - Double precision word fetch from stack

1st - First word received on a multi-word operation

STACK OUTPUT REGISTER (SO) - The output of the Storage Unit Queue

APR - Address Present (Not Used)

WAT - Wait for EU store operation

STR - Store (set for store or overwrite, reset for fetch)

PRO - Protect (set for store, reset for overwrite).

FMF - Fetch Memory Fail Register

CHN - Channel number used to address MCM (used with special ops)

LMT - Set Memory Limits

INH - Set Memory Inhibits.

LAM - Load Associative Memory.

Q-LOC - QL1-0 - Location in the E.U. Data Queue, passed from the PCU.

EWR - Write into the EU Write Register

DP - Double precision word fetch from stack.

LENGTH 7-5 - Number of words to be transferred.

CHNL# 4-1 - MCM number.

OVF - Not Used.

ADDER SECTION

Row 6

CONTROL - Control bits for the address adder.

DT1,0 - Address adder timing

BYE - E.U. is busy with the address adder.

BYP - PCU is busy with the address adder.

RCY - Read cycle

ACY - Add cycle

EXC - Extra cycle

WCY - Write cycle

SWR - Save Write residue

SAC - Select address couple which is used with a name call or value call.

ADD - Add one

ADW - Adder to Display Write Register.

CDW - Complement the Display Write Register.

PGL - Not Used

AUO - Address adder overflow

AZF - Address adder output's all zeros

ARE - Address request for EWR

EU READ PT (ERP5-0) - The address adder read pointer for the EU which allows the EU to access the addressible registers.

PCU READ PT (PRP5-0) - The address adder read pointer for the Program Unit which allows the PCU to access the addressible registers.

WRITE PT (DWP5-0) - The address adder write pointer. Only the EU can write into the addressible registers.

SI

APR - Set to allow a write into the Storage Unit Queue.

WAT - Wait on a Store operation. The EU is generating the information to be written based on a prior read of that location. Action of this variety would occur if an IRW was encountered on a protected write.

LAM - Load Associative Memory which indicates that a fetch is in process.

SI

Q-LOC (bits 11,10) - The queue location in the E.U. Data Queue.

SI

DP - Double precision

OVF - Overflow (Not Used)

SD POINTER (SD)

R1,0 - SDR1,0 is the Storage Unit data pointer for read operations.

W1,0 - SDW1,0 is the Storage Unit data pointer for write operations.

SQ POINTER (SQ)

W2-0 - SQW2-0 - The Storage Operator Queue Write pointers.

R2-0 - SQR2-0 - The Storage Operator Queue read pointers.

The Storage Operator Queue contains the S.U. operator control bits and addresses.

STACK SECTION

Row 7 - Row 27 Display Selection

The seventh row of indicators is used to display the contents of either row 7 or row 27. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the seventh row of indicators and which is labeled SR/SAR/MISC - SLR/LOSR/MISC.

Row 7

S REGISTER (SR)

Bits 21,20 - SR21,20 are the "S" Register residue.

Bits 19-0-SR19-0 is the "S" Register which contains the main memory address of the top of stack.

STACK ADDRESS REGISTER (SA)

Bits 21,20 - SA21,20 are the Stack Address Register residue.

Bits 19-0 - SA19-0 is the Stack Address Register which contains the main memory address of the lowest word in the stack buffer.

MISC BITS

RIW - Repeat 1 word - used when pushing stack buffer to memory and 4th word is double precision.

RPG - Remember Purge. Remembers first purge after an exit op. Causes purge of associative memory.

Row 27

STACK LINK REGISTER (SL)

Bits 21,20 - SL21,20 are the Stack Link Register residue.

Bits 19-0 - SL19-0 is the Stack Link Register which contains the main memory address of the lowest word in the stack buffer which has not been written to main memory.

LIMIT OF STACK REGISTER (LO)

Bits 21,20 - LO21,20 are the Limit of Stack Register residue.

Bits 19-0 - LO19-0 is the Limit of Stack Register which contains the main memory address of the maximum limit of the stack's assigned area.

MISC BITS

LC05 - The most significant bit of the LC pointers which are located in row 28 in bits 25-22.

Row 8 - Row 28 Display Selection

The eighth row of indicators is used to display the contents of either row 8 or row 28. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the eighth row of indicators and which is labeled MAR/CONT - FR/KPT.

Row 8

MEMORY ADDRESS REGISTER (MA)

Bits 21,20 - MA21,20 are the Memory Address Register residue.

Bits 19-0 - MA19-0 is the Memory Address Register which contains the address which will be transferred to the Comm address for main memory accesses.

STACK CONTROL

EBK - E.U. busy with the stack.

SBK - S.U. busy with the stack.

BBK - Buffer busy with the stack.

KP3,KP2,KP1 - Stack phases 3, 2, an 1

KT1,KT0 - Stack Time 1 and 0

KHD - Stack hold

KEC - Stack end of cycle

KRC - Stack requests Comm.

PSH - Push

POP - Pop

PRG - Purge

RET - Return or set processor register for the "S" Register.

BST - Not Used

KRL - Stack read local (KLC is valid)

KLC - Stack local. MAR is less than S and greater than SLR.

KAS - Stack above S

RPT - Not Used

FIL - Fill

EMT - Empty

T2B - Top pointer is two away from the bottom pointer.

TEB - Top pointer is equal to the bottom pointer.

TSR - Top of stack read (from memory to the stack).

TSW - Top of stack write (from the stack to memory).

SBYP - Storage Unit bypass. The EU is making a fetch and is bypassing the storage unit queue.

Row 28

F REGISTER (FR)

Bits 21,20 - FR21,20 are the F Register residue.

Bits 19-0 - FR19-0 is the F Register which points at the current Mark Stack Control Word.

STACK POINTERS

ISU - Inhibit stack underflow from setting fault bit (not presently used).

KWT - Stack write

LC04-0 - Length count.

LR04-0 - Local read pointer.

LK04-0 - Link pointer which contains the address of the Stack Buffer Location which corresponds to the SLR setting.

TP04-0 - Top pointer which contains the address of the Stack Buffer Location which corresponds to the S setting.

BT04-0 - Bottom pointer which contains the address of the Stack Buffer location which corresponds to the SAR setting.

PROGRAM CONTROL UNIT SECTION

Row 9 - Row 29 Display Selection

The ninth row of indicators is used to display the contents of either row 9 or row 29. The selection of the row to be displayed is made through use of a toggle switch which is located on the right hand side of the panel adjacent to the ninth row of indicators and which is labeled PUR/PLR/RE/RO - DWR/DRR/SSL.

Row 9

PROGRAM UPPER REGISTER (PU)

Bits 19-0 - PU19-0 is the Program Upper Register which contains the main memory address of the next word to be loaded into the Program Buffer.

Bits 21,20 - PU21,20 are the Program Upper Register residue.

PROGRAM LOWER REGISTER (PL)

Bits 21,20 - PL21,20 are the Program Lower Register residue.

Bits 19-0 - PL19-0 is the Program Lower Register which contains the main memory address of the oldest active entry in the Program Buffer.

READ EVEN (PEB3-0) - A pointer to the even word in the Program Buffer which is input to the Program Unit barrel selection logic.

READ ODD (POB3-0) - A pointer to the odd word in the Program Buffer which is input to the Program Unit barrel selection logic.

Row 29

DISPLAY WRITE REGISTER (DW)

Bits 19-0 - DW19-0 is the Display Write Register which is the input register for all addressible registers. The DWR is one of the inputs to the address adder and is the location into which the "hard" registers are manually read.

Bits 21,20 - DW21,20 are the Display Write Register residue.

DISPLAY READ REGISTER (DR)

Bits 21,20 - DR21,20 are the Display Read Register residue.

Bits 19-0 - DR19-0 is the Display Read Register which is the output register of the addressible registers.

SSL - (SSL2-0) - Save storage length which is used to save the fetch length to recycle through local memory on a multi-word fetch where the first part of the information is in main memory and the remainder is in local memory.

Row 10

PROGRAM ADDRESS REGISTER (PA)

Bits 19-0 - PA19-0 is the Program Address Register which contains the main memory address of program code only when a change of direction occurs. The address is then transferred to the Program Upper Register only if a branch point is found to be non-local.

Bits 21,20 - PA21,20 are the Program Address Register residue.

PROGRAM BUFFER CONTROL

PWP - PWP4-0 - The Program Write Pointer for the Program Buffer when in normal mode.

RPD - Indicates that the Program Read Pointer should be decremented.

PWE4,PWE3 - The Program Write Pointer which is used in place of PWP when in Edit Mode.

BK2-0 - The number of blocks of normal code which are in the Program Buffer.

BR4,BR3 - Pointer to the block of code that is associated with the Program Lower Register.

PRC - Program Buffer requests Comm Unit

TUL - Transfer program upper to program lower

IPU - Increment program upper

PROK - Program residue OK

CPA - Count Program Address Register

PRI - Pulse switch flip-flop

SNC - Sync

STR - Start

ERC - Edit read control for Program Buffer.

EWC - Edit write control for Program Buffer.

Row 11

EDT - Processor is in the table option of Edit Mode.

EDS - Processor is in the single option of Edit Mode.

EUP - Edit Mode is in update variation.

ESM - Edit Mode is in double pointer variation.

LEXIC LEVEL (LL4-0) - Contains the current Lexic Level.

OKLQ - Operator and K-and-L Queue Write F.F.

LLW (LLW4-0) - Lex Level write which is the input to the Lex Level Queue where, under some conditions, the Lex Level is stored.

SAVE SYLL (SSR4-0) - The Syllable Save Register is used as interim storage on transfer from the EU to the PCU and is also used to save the normal syllable when entering Edit Mode. The Just two bits of this register (SSR4,SSR3) are the syllable residue, and the remaining three bits (SSR2-0) contain the syllable.

DATA Q - EU Data Queue

DQMT - Data Queue empty

QER - E.U. Data Queue error.

QDV - E.U. Data Queue valid.

DA1-0 - A two bit index into the EU Data Queue. This is the origin of all similar indicies into the EU Data Queue.

WLS - EU Data Queue write least significant.

NAME CALL - Name call concatenation control flip-flops.

NCF - A name call has been concatenated with either INDX, NXLV, or NXLN.

NCE - Name call - enter concatenation has been accomplished.

NCS - Name call - store concatenation has been accomplished.

PNE - Program Index Register error.

IPN - Allows a special count of the Program Index Register when in Vector Mode.

VRN1,0 - Variant residue.

AR1,0 - Address couple residue.

IEP - IEP2-0. Parity bits for syllables located in the IER.

IDP - IDP2-0. Parity bits for syllables located in the IDR.

RPC - Remember program count.

OEA,OEB,OEC - Odd/even flip-flops for the Program Buffer.

BARREL SELECT (BS5-0). The shift controls for the Program Buffer.

Row 12

ORDER CODE WRITE (OW)

ESA,ESB - Indicate the state of the stack at the beginning of the program operator.

RPT - The E.U. report bit which causes the E.U. to notify the PCU when it's done with the micro-op.

END - Indicates the end of the final micro-op for a program operator. Final command, final routine should also be true.

Bits 7-0 - OW7-0 is the Order Code Write Register (OW) which receives the micro operators that have been generated by the PCU. The output from the OW Register either goes into the E.U. Operator Queue or goes directly into the operator registers of all families.

DGC - Disable generated code to the E.U.

OQW - E.U. operator queue write.

QW - QW2-0 are write pointers for the E.U. operator queue.

STACK (SKA,SKB) - The stack environment at the conclusion of a program operator. SKA and SKB will be transferred to IMA and IMB which are transferred to ESA and ESB in the OW Register.

HOLD CONDITIONS

EDN - Indicates that the EU is done. It is set from RPT (Report) and is used for synchronization between the PCU and EU.

QFL - The EU Operator Queue is full.

CRE - Comm. Unit request for use of the E.U. Queue Write Register (EWR).

SRE - Storage Unit request for use of the EWR.

ERE - Execution Unit request for use of the EWR.

NOTE

EWR is the input to the Data Queue in the Execution Unit.

DQF - E.U. Data queue full.

PAE - E.U. has completed a predetermined accidental entry.

MRK - E.U. has completed a Mark Stack operation.

CDN - Comm Unit has completed all requests for service.

QEM - E.U. Operator Queue is empty.

RPA - Reset PWA flip-flop.

PBB - Program Buffer busy with replenishment.

STG - Remember string operator.

TO-1 - Timing for PCU.

HL2 - Master hold flag which disables time zero strobe distribution.

TO-2 - Timing for PCU.

HL3 - Master hold flag which disables time zero strobe distribution.

TO-3 - Timing for PCU.

T1 - Timing for PCU.

ISO - Inhibit stack overflow from setting fault bit.

VSI - Involved in loading the control bits associated with the Storage Unit.

LSI - Load Storage Unit input address (queue input register).

KDA - Stack disable.

MSK - Master sync.

REP COUNTER (RPC3-1) - Extensions of the Phase Counter.

Row 13

SUBROUTINES - Hardware subroutines

EUT - A EUIT indication in the PCU set by the EU so that a hardware subroutine can be initiated.

ACT - Hard routine for re-execution of instructions for interrupts.

CKL - Length check routine in Vector Mode.

DOB - Hardware routine for execution of dynamic operand branch.

EDI - Edit interrupt subroutine

EED - Hardware routine for leaving Edit Mode due to an interrupt.

ENT - Hardware routine for Enter Junction during an interrupt.

IBR - Interrupt Branch condition in non-Table Edit Mode.

INT - Hardware routine for interrupt handling

LOD - Hardware routine for initialization of the Program Buffer.

MNE - Hardware routine to accomplish the following sequence: Mark Stack, Name call, Enter.

MOV - Hardware routine to accomplish a Move Stack operation.

PAS - Hardware routine to accomplish a Pause Junction.

RST - Restart Execution Unit in preparation for interrupt.

SRG - Hardware routine for string operator interrupt processing.

NEO - Non-existent order code.

ADP - D8, when set, causes issuance of a fetch-to-stack (Pop).

ADM - DA - When set, causes issuance of a push.

HOLD LOGIC

RPT - Hold for report from E.U.

DEC - Disable communication to the E.U.

PRE - Program Unit requests use of the Execution Unit Write Register.

PTG - Program word has a tag error.

PPE - Program word has a parity error.

LDQ - Load Execution Unit Data Queue

HAE - Hold up program control for a predetermined accidental entry.

HFM - Hold up Program control until Execution Unit completes mark.

CLQ - Clear all queues for a change in program division.

HSI - Hold up Program control as the processor is in Single Instruct.

PBA - Program buffer available.

PWA - Program Control Unit requests use of the address adder.

INH - Inhibit Program Buffer fetches from main memory.

HFP - Hold for pack. This flip-flop is set when a pack operator is detected. Unlike other holds, HFP does not enable the hold immediately. The hold is enabled only if the next operator is a string operator.

HL1 - Master hold flag which disables time zero strobe distribution.

SWG - Something wrong flip-flop. If set, then whatever phase we are in as determined by the phase counter becomes a special phase. In effect, this causes hesitation in normal operation due to an exception condition (two sequential string operators).

BGN - Begin first phase of instruction.

PHASE COUNTER (PHF-0). - Indicates phase of the program operator.

Row 14

I E CONTROL - Instruction Execution Register (IER) Control.

IMA - Intermediate stack condition for the "A" operand.

DEE - Decode Edit Mode operators in the IER.

DVE - Decode Variant Mode operators in the IER.

IMB - Intermediate stack condition for the "B" operand.

INSTRUCTION EXECUTE REGISTER (IER23-0) - A three syllable register which receives the program operator from the IDR and decodes it into micro-operators. In effect, this is the execution register for a program operator.

SQE - A disable flip-flop for the IER for sequencing. Sequencing is the time period during which the processor is in a hardware subroutine.

VEC - A flip-flop indicating Vector Mode.

APC - Adjust program count for presence bit interrupt.

PROGRAM INDEX CURRENT (PC)

Bits 17,16 - PC17,16 is program index current residue.

Bits 15-0 - PC15-0 is program index value for the word currently the IER which, when added to the PBR gives the absolute memory address.

C SYLL (CS2-0) is the syllable count for the IER. count for the IER.

Row 15

ID CONTROL - Instruction Decode Register (IDR) control bits.

LID - Load the ID. When set, the barrel output is transferred to the IDR and the information in the

IDR is transferred to the IER. PN and NS are also transferred to PC and CS respectively.

DED - Decode Edit Mode operators in the IDR.

DVD - Decode Variant Mode operators in the IDR.

LID - Duplicate of the first LID, for Loading purposes.

INSTRUCTION DECODE REGISTER (IDR23-0) - The IDR is a three syllable register which is normally considered to be the "look ahead" station. The IDR is decoded for barrel shifts and counts for "fast" program operators. A combination of IDR and IER action is necessary for the "slower" operators. Decoding of the IDR also provides the initial set-up for stack maintenance and determines if an operator occurred which requires concatenation.

SQD - A disable flip-flop for the IDR for sequencing. Sequencing is the time period during which the processor is in a hardware subroutine.

TIR - The Table Index Register flag which, when true, indicates that the index and syllable in PN and NS are a table index for Edit Mode rather than an index from the PBR.

NPR - Designates an alternate PIR. When NPR is true and an interrupt occurs, this indicates that the PIR queue should not be used, rather an alternate PIR (APIR hex address 39) should be used.

PROGRAM INDEX NEXT (PN).

Bits 17,16 - PN17,16 are the Program Index Next residue.

Bits 15-0, PN15-0 - The index value for the word currently in the IDR, which, when added to the PBR gives the main memory address.

N SYLL (NS2-0) is the next syllable count for the IDR.

PANEL 1 SWITCHES (RIGHT-HAND PANEL)

POWER

OFF - Removes power from the CPM.

ON - Applies power to the CPM.

READY - Indicates that the powering-up sequence is complete.

STATUS

ON LINE - The CPM is in on-line operation. All control switches, with the exception of power, are disabled.

TEST - The CPM is in Test operation. All control switches are enabled.

TEST

STORAGE - Sets or resets the flip-flops and indicators as specified through the toggle and thumb wheel switches.

LAMP-Sets or indicators as specified through the thumb wheel switches.

FANS-FAULT - Indicates that the CPM has sensed a fan failure, and has been automatically powered down.

TG2 - Not wired

PB2 - Not wired

PB1 - Used in conjunction with PLS local buffer control switch to cause a purge of the stack buffer.

TG1 - Not wired

CLEAR - Zeros the field selected through the Thumb Wheel switches.

PAN - Panel number.

ROW - Indicator row which is printed on the right hand margin of the panel.

GRP - Group. A normal group (1) consists of ten indicators, thus group 0 consists of bits 9-0. Group 9 specifies that action will be taken on the entire selected row.

LOAD - The contents of the toggle switches will be loaded (OR'd) into the location specified through the thumb wheel switches.

SINGLE PULSE

ON-OFF - Enables a disables single pulse action. If this switch is on, the Special Function switch on panel 1 must also be set.

Push Button - Used for single pulsing. When this switch is depressed, one sixteen-megacycle clock is generated.

SERIAL MODE - Causes the unit to wait until the EU completes each micro-op before it is given another one. The micro-op thus is taken directly from the OW Register rather than the E.U. Operator Queue.

CONDITIONAL HALT - This will cause a halt if the conditional halt operator occurs. Processing may be continued, dependent on the situation. by pressing the Start switch.

ADDRESS HALT - Not wired.

PROGRAM HALT - This will cause a halt if Program Index Current and C Syll (Panel 1 row 14 Bits 18-0) are equal to the value selected in toggle switches 18-0.

STACK DISABLE - When set, this forces the unit to go to main memory for each fetch.

ASM DISABLE - Inhibits the use of Associative Memory.

SINGLE INST. - Allows a single program operator to be executed each time Start is depressed. This switch is also used to temporarily stop the processor.

REPEAT PROGRAM - Causes the CPM to cycle through the Program Buffer without obtaining more code from main memory.

CONTROL CLEAR - Clears all "hard" registers to the reset state.

START - Resumes execution after a Halt condition.

PANEL OPERATIONS

SETTING/RESETTING OF INDICATORS

The indicators and their associated flip-flops can be manually set or reset either from the CPM display panels or from the MDU. Selection of a row of indicators and a specific group within the row is made through four thumbwheel switches which are located on the bottom portion of the right hand panel, panel 1. The switch allows the selection of a Panel (1 or 2), Row (1-15, 21-23, 27-29, 34), and Group (0-5, 9), "Group" is a group of ten indicators numbered from 0 through 6 from right to left. A group value of nine indicates that the entire row will be acted on.

Once that the row has been selected, it can be modified through the 51 toggle switches at the bottom of each panel. The Clear button, located immediately to the left of the Thumb Wheel switches, causes zeros to be loaded into the selected row. The Load button, located immediately to the right of the Thumb Wheel switches, causes the contents of the toggle switches to be "OR"ed with the appropriate flip-flops. It is thus necessary to clear an area and to load it with new values to RESET a selected indicator.

LAMP TEST

NOTE

The Lamp Test is used to test the indicators only. The flip-flops associated with the indicators are not set.

1.	STATUS SWITCH	Place in the TEST position.
2.	TEST (SWITCHES)	Place the LAMP switch in the ON position.
3.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=N/A, Group=0
4.	LOAD SWITCH	PUSH. Indicators on Panel 1 in toggle switch positions 9-0 of all rows should light.
5.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=N/A, Group=1
6.	LOAD SWITCH	Push. Indicators on Panel 1 in toggle switch positions 19-10 of all rows should light.
7.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=N/A, Group=2
8.	LOAD SWITCH	Push. Indicators on Panel 1 in toggle switch positions 29-20 of all rows should light.
9.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=N/A, Group=3
10.	LOAD SWITCH	Push. Indicators on Panel 1 in toggle switch positions 39-30 of all rows should light.
11.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=N/A, Group=4
12.	LOAD SWITCH	Push. Indicators on Panel 1 in toggle switch positions 49-40 of all rows should light.
13.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=N/A, Group=5

14.	LOAD SWITCH	Push. Indicators on Panel 1 in toggle switch positions 51, 50 of all rows should light.
15.	THUMB WHEEL SWITCHES	Set(to Panel=2, Row-N/A, Group=0
16.	LOAD SWITCH	Push. Indicators on Panel 2 in toggle switch positions 9-0 of all rows should light.
17.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=N/A, Group=1
18.	LOAD SWITCH	Push. Indicators on Panel 2 in toggle switch positions 19-10 of all rows should light.
19.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=N/A, Group=2
20.	LOAD SWITCH	Push. Indicators on Panel 2 in toggle switch positions 29-20 of all rows should light.
21.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=N/A, Group=3
22.	LOAD SWITCH	Push. Indicators on Panel 2 in toggle switch positions 39-30 of all rows should light.
23.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=N/A, Group=4
24.	LOAD SWITCH	Push. Indicators on Panel 2 in toggle switch positions 49-40 of all rows should light.
25.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=N/A, Group=5
26.	LOAD SWITCH	Push. Indicators on Panel 2 in toggle switch positions 51, 50 of all rows should light.
27.	TEST (SWITCHES)	Return the LAMP switch to the OFF position.

STORAGE TEST

NOTE

The Storage Test sets or resets both the indicators and their associated flip-flops.

It is therefore necessary to either de-commit the CPM before the test and re-commit it following the TEST or Halt/Load following the TEST.

1.	STATUS SWITCH	Place in the TEST position.

2.	SINGLE PULSE (Panel 2)	Place in the ON position.
3.	TEST (SWITCHES)	Place the SORAGE switch in the ON position.
4.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=N/A, Group=9
5.	PANEL 1 CONTROL CLEAR	Push. All wired indicators on Panel 1 should be OFF (reset).
6.	PANEL 1 TOGGLE SWITCHES	Place all switches in the UP (set) position.
7.	LOAD SWITCH	All wired indicators on panel 1 should be ON (set).
8.	PANEL 1 CONTROL CLEAR	Push. All wired indicators on panel 1 should be OFF (reset).
9.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=N/A, Group=9.
10.	PANEL 2 CONTROL CLEAR	Push. All wired indicators on Panel 2 should be OFF (reset).
11.	PANEL 2 TOGGLE SWITCHES	Place all switches in the UP (set) position.
12.	LOAD SWITCH	Push. All wired indicators on Panel 2 should be ON (set).
13.	PANEL 2 CONTROL CLEAR	Push. All wired indicators on Panel 2 should be OFF (reset).
14.	TEST (SWITCHES)	Restore the STORAGE switch to the OFF position.
15.	SINGLE PULSE (Panel 2)	Restore to the OFF position.

NOTE

The CPM must now either be re-committed or Halt/loaded.

PROGRAM BUFFER READ

1.	STATUS SWITCH	Place in TEST position.
2.	SINGLE INST	Place in ON position.
3.	REPEAT PROGRAM	Place in ON position.
4.	PANEL 2, ROW 1-21 DISPLAY SELECTION	Place in the UP position for display of the EWR.
5.	PANEL 2, ROW 1	Record the contents of the EWR.
6.	PANEL 2, ROW 4, BIT 90	Record the setting of th EW Data Valid bit (DV of the EU Write Register extras).
7.	PANEL 1, ROW 9-29 DISPLAY SELECTION	Place in the UP position for display of the Program Lower Register. Read Even, and Read Odd.
8.	PANEL 1, ROW 9	Record the contents of the last two bits of the Program Lower Register, and the entire contents of Read Even and Read Odd.
9.	PANEL 1, ROW 11	Record the contents of RPC, the Program Buffer odd/even flip-flops, OEA, OEB, and OEC, and Barrel Select (BS5-0).
10.	LOCAL BUFFER CONTROL	Place PRB switch in the UP position.
11.	LOCAL BUFFER CONTROL	Place R/W switch in the UP position.
12.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=9, Group=0.
13.	CLEAR SWITCH	Push to zero Program Even and Program Odd.

NOTE

The Program Buffer is a 32 word storage area which is divided into halves, one half containing the even address and the other containing the odd addresses. The values of Program Even and Program Odd are therefore from 0 through 15.

NOTE

As soon as addresses are placed in Program Even and Program Odd the output appears in the EWR Register on panel 2. If the odd address is desired, OEA must be set; otherwise it must be reset.

14. PANEL 1 TOGGLE SWTCHES — Set switches 7-4 to the Program Even address and switches 3-0 to the Program Odd address.

15. LOAD SWITCH — Push to load the addresses into Program Even and Program Odd.

Either the Even or Odd output will immediately appear in EWR.

NOTE

If OEA, OEB, and OEC have the desired setting please go to step 24.

NOTE

If OEA, OEB, and OEC are set, causing a read of the odd Program Buffer, perform steps 17, 18, 22, 23.

NOTE

If OEA, OEB, and OEC are RESET, causing a read of the even Program Buffer, perform steps 17, 19-23.

16. THUMB WHEEL SWITCHES — Set to Panel=1, Row=11, Group=0.

17. CLEAR SWITCH — Push to zero RPC, OEA, OEB, OEC, and BS5-0.

A new output will appear in the EWR as soon as the odd/even flip-flops are reset.

18. PANEL 1 TOGGLE SWITCHES — Set switches 8, 7, and 6.

19. LOAD SWITCH — Push to set the odd-even flip-flops.

A new output will appear in the EWR as soon as the odd/even flip-flops are set.

20. CLEAR SWITCH — Push to zero RPC, OEA, OEB, OEC, and BS5-0.

21.	PANEL 1 TOGGLE SWITCHES	Set switches 9-0 to the values recorded in step 9.
22.	LOAD SWITCH	Push to restore the original contents to RPC, OEA, OEB, OEC, and BS5-0.

NOTE

End of special odd/even flip-flops processing.

23.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=9, Group=0.
24.	CLEAR SWITCH	Push to clear the last two bits of PL and all of PEB and POB.
25.	PANEL 1 TOGGLE SWITCHES	Set switches 9-0 to the values recorded in step 8.
26.	LOAD SWITCH	Push to restore the original contents of PL, PEB, and POB.
27.	LOCAL BUFFER CONTROL	Restore R/W switch to the DOWN position.
28.	LOCAL BUFFER CONTROL	Restore PRB switch to the DOWN position.
29.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=1, Group=9.
30.	CLEAR SWITCH	Push to zero the EWR.
31.	PANEL 2 TOGGLE SWITCHES	Set switches 51-0 to the values recorded in step 5.
32.	LOAD SWITCH	Push to restore the original contents of the ERW.

NOTE

If the EW Data Valid bit has the same value as that obtained in step 6, please go to step 41.

NOTE

If EWDV is presently not set perform steps 34, 35, and 36.

NOTE

If EWDV is presently set, perform steps 34, 37-40.

33.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=4, Group-4.

34.	PANEL 2 TOGGLE SWITCHES	Set switch 40, all other switches must be reset (down).
35.	LOAD SWITCH	Push to set EWDV.
36.	PANEL 2, ROW 4,	Record the settings of ME49-45, NT, NC, NV, and PV.
37.	CLEAR SWITCH	Push to zero EWDV.
38.	PANEL 2 TOGGLE SWITCHES	Set switches 49-41 to the values recorded in step 37. Switch 40 must be down (FALSE).
39.	LOAD SWITCH	Push to restore the original contents of ME49-45 NT, NC, NV, PV, and DV.

NOTE

END OF SPECIAL EWR DATA VALID PROCESSING.

40.	REPEAT PROGRAM	Restore to OFF position.
41.	SINGLE INST	Restore to OFF position.
42.	START	Push to continue processing.

PROGRAM BUFFER WRITE

1.	STATUS SWITCH	Place in TEST position.
2.	SINGLE INST	Place in ON position.
3.	LOCAL BUFFER CONTROL	Place PRB switch in UP position.
4.	LOCAL BUFFER CONTROL	Place R/W switch in DOWN position.
5.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=10, Group=2.
6.	PANEL 1, ROW 10	Record contents of PWP, RPD, PWE4, PWE3, and BK2.
7.	CLEAR SWITCH	Push to zero bits 29-20 in row 10.
8.	PANEL 1 TOGGLE SWITCHES	Set switches 29-244 to the desired Program Buffer address. The allowable values are from 0 through 31.
9.	LOAD SWITCH	Push to load toggle switch settings into PWP.

10.	PANEL 1, ROW 1-21 DISPLAY SELECTION	Place in the UP position for the Input Register display.
11.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=1, Group=9.
12.	PANEL 1, ROW 1	Record contents of the Input Register.
13.	CLEAR SWITCH	Push to zero the Input Register.
14.	PANEL 1 TOGGLE SWITCHES	Set switches 51-0 to the desired value for entry into the Program Buffer. Bit 51 (the parity bit) must be correctly set to obtain good parity (odd).
15.	LOAD SWITCH	Push to load toggle switch settings into the Input Register.
16.	LOCAL BUFFER CONTROL	Toggle PLS once to write into the Program Buffer. PWP will be incremented.

NOTE

To write into the next sequential Program Buffer address, repeat steps 13-16.

17.	CLEAR SWITCH	Push to zero the Input Register.
18.	PANEL 1 TOGGLE SWITCHES	Set switches 51-0 to the values recorded in step 12.
19.	LOAD SWITCH	Push to restore the original contents of the Input Register.
20.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=10, Grou=2.
21.	CLEAR SWITCH	Push to zero PWP, RPD, PWE4, PWE3, and BK2.
22.	PANEL 1 TOGGLE SWITCHES	Set switches 29-20 to the values recorded in step 6.
23.	LOAD SWITCH	Push to restore the original contents of PWP, RPD, PWE4, PWE3, and BK2.
24.	LOCAL BUFFER CONTROL	Restore PRB switch to DOWN position.
25.	SINGLE INST	Push to turn OFF.
26.	START	Push to start processing.

STACK BUFFER READ

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.
3.	PANEL 1 ROW 1-21 DISPLAY SELECTION	Place in the UP position for display of row 1.
4.	PANEL 1 ROW 8-28 DISPLAY SELECTION	Place in the DOWN position for display of row 28.
5.	PANEL 1 ROW 1	Record the setting of all indicators in the row.
6.	PANEL 1 ROW 28	Record the setting of PT04-0 and BT04-0.
7.	LOCAL BUFFER CONTROL	Place the STK switch in the UP position.
8.	LOCAL BUFFER CONTROL	Place the R/W switch in the Up position.
9.	THUMB WHEEL SWITCHES	Set to Panel=1, Row-28, Group=0.
10.	CLEAR SWITCH	Push to zero BT04-0.
11.	PANEL 1 TOGGLE SWITCHES	Set switches 4-0 to the Stack Buffer address.
12.	LOAD SWITCH	Push to load the address into BT04-0.
13.	LOCAL BUFFER CONTROL	Toggle the PLS switch once. The output will appear in the Input Register.

NOTE

After the read has been performed, BT is automatically decremented by one. A read of the next stack buffer word can be done by toggling PLS.

14.	CLEAR SWITCH	Push to zero BT04-0.
15.	PANEL 1 TOGGLE SWITCHES	Set switches 4-0 to the values recorded in step 6.
16.	LOAD SWITCH	Push to restore the original settings of PT04-0 and BT04-0.
17.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=1, Group=9.

18.	CLEAR SWITCH	Push to zero the Input Register.
19.	PANEL 1 TOGGLE SWITCHES	Set switches 51-0 to the values recorded in step 5.
20.	LOAD SWITCH	Push to RESTORE the original contents of the Input Register.
21.	LOCAL BUFFER CONTROL	Restore R/W switch to the DOWN position.
22.	LOCAL BUFFER CONTROL	Restore STK switch to the DOWN position.
23.	SINGLE INST SWITCH	Resotre to the OFF position.
24.	START	Push to continue.

STACK BUFFER WRITE

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.
3.	LOCAL BUFFER CONTROL	Place the STK switch in the UP position.
4.	PANEL 1 ROW 1-21 DISPLAY SELECTION	Place in the UP position for the display of row 1.
5.	PANEL 1 ROW 8-28 DISPLAY SELECTION	Place in the DOWN position for the display of row 28.
6.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=28, Group=0.
7.	PANEL 1 ROW 28	Record the settings of TP04-0 and BT04-0 (toggle switch positions 9-0).
8.	CLEAR SWITCH	Push to zero BT04-0.
9.	PANEL 1 TOGGLE SWITCHES	Set switches 4-0 to the desired stack buffer address.
10.	LOAD SWITCH	Push to set BT04-0 to the values specified in the toggle switches.
11.	THUMB WHEEL SWITCHES	Set to Panel=1, Row-1, Group=9.
12.	PANEL 1 ROW 1	Record the settings of all indicators in the row. row.
13.	CLEAR SWITCH	Push to zero the Input Register.

14.	PANEL 1 TOGGLE SWITCHES	Set switches 51-0 for the information to be written into the stack buffer, Parity (odd) must be maintained.
15.	LOAD SWITCH	Push to set the contents of the Input Register to that of the toggle switches.
16.	LOCAL BUFFER CONTROL	Toggle the PLS switch once to write into the stack buffer.

NOTE

The buffer address is incremented following the write; therefore, to write the next location, repeat steps 13-16.

17.	CLEAR SWITCH	Push to zero the Input Register.
18.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in Step 12.
19.	LOAD SWITCH	Push to restore the original contents of the Input Register.
20.	THUMB WHEEL SWITCHES	Set to Panel=1, Row-28, Group=0.
21.	CLEAR SWITCH	Push to zero BT04-0.
22.	PANEL 1 TOGGLE SWITCHES	Set switches 9-0 to the values recorded in step 7.
23.	LOAD SWITCH	Push to restore the original settings of TP04-0 and BT04-0.
24.	LOCAL BUFFER CONTROL	Restore the STK switch to the DOWN position.
25.	SINGLE INST SWITCH	Restore to the OFF position.
26.	START SWITCH	Push to continue.

DISPLAY BUFFER-ADDRESSIBLE REGISTERS

The following registers can be accessed through the Display Buffer:

Address (Decimal)	Address (Hex)	Register Name	Register Usage
0-31	0-1F	D[N]	Display Registers
33	21	SIR	Source Index Register
34	22	DIR	Destination Index Register
35	23	TIR	Table Index Register
37	25	BOSR	Base of Stack Register
39	27	BUF	Scratch Register
48	30	PBR	Program Base Register
49	31	SBR	Source Base Register
50	32	DBR	Destination Base Register
51	33	TBR	Table Base Register
53	35	SNR	Current Stack Number
54	36	PDR	Current Segment Descriptor Index
55	37	TEMP	Scratch
56	38	ADZ	Alternate D[0]
57	39	APIR	Alternate Program Index Register
58	3A	ALL1	All ones

DISPLAY BUFFER READ

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.
3.	PANEL 1 ROW 9-29 DISPLAY SELECTION	Place in the DOWN position for display of the DRR.

4.	PANEL 1 ROW 29	Record the setting of all indicators in the row.
5.	LOCAL BUFFER CONTROL	Place the DSP switch in the UP position.
6.	THUMB WHEEL SWITCHES	Set to Panel = 1, Row = 6, Group = 9.
7.	Panel 1 Row 6	Record the setting of all indicators in the row.
8.	CLEAR SWITCH	Push to zero the EU Read Pointer (ERP).
9.	PANEL 1 TOGGLE SWITCHES	Set switches 34-29 to the hexadecimal address of the desired register.
10.	LOAD SWITCH	Push to set ERP to the toggle switch values.
11.	LOCAL BUFFER CONTROL	Place the R/W switch in the UP position.

NOTE

Intermation will appear in the DRR when the R/W switch is placed in the UP position. If another register is to be read, repeat steps 8-10, information will appear in DRR when the new address is loaded.

12.	LOCAL BUFFER CONTROL	Restore the R/W switch to the DOWN position.
13.	CLEAR SWITCH	Push to zero the ERP.
14.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in step 7.
15.	LOAD SWITCH	Push to restore the original settings in row 6.
16.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=29, Group=9
17.	CLEAR SWITCH	Push to zero the DRR.
18.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in step 4.
19.	LOAD SWITCH	Push to restore the original contents of row 29.
20.	LOCAL BUFFER CONTROL	Restore the DSP switch to the DOWN position.

21.	SINGLE INST SWITCH	Restore to the OFF position.
22.	START SWITCH	Push to continue processing.

DISPLAY BUFFER WRITE

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.
3.	PANEL 1 ROW 9-29 DISPLAY SELECTION	Place in the DOWN position for display of the DWR.
4.	LOCAL BUFFER CONTROL	Place the DSP switch in the UP position.
5.	THUMB WHEEL SWITCHES	Set to Panel=1, Row-6, Group=9.
6.	PANEL 1 ROW 6	Record the setting of all indicators in the row.
7.	CLEAR SWITCH	Push to zero the Display Write Pointer (DWP).
8.	PANEL 1 TOGGLE SWITCHES	Set switches 21-17 to the Hexadecimal address of the desired register.
9.	LOAD SWITCH	Push to set DWP from the toggle switches.
10.	THUMB WHEEL SWITCHES	Set to Panel=1, Row-29, Group=9.
11.	PANEL 1 ROW 29	Record the settings of all indicators on the row.
12.	CLEAR SWITCH	Push to zero the Display Write Register (DWR).
13.	PANEL 1 TOGGLE SWITCHES	Set switches 51-32 for the information to be written into the selected register.
		Set switches 31, 30 for the residue for the information.

14.	LOAD SWITCH	Push to write the toggle switch settings into DWR.
15.	LOCAL BUFFER CONTROL	Toggle the PLS switch once to write into the selected register. DWP will be incremented following the write.
		NOTE
	To write into steps 12-15.	the next display D±N1 register, repeat
16.	CLEAR SWITCH	Push to zero row 29.
17.	PANEL 1 TOGGLE SWITCHES	Set switches 51-0 to the values recorded in step 11.
18.	LOAD SWITCH	Push to restore the original settings to Panel 1 row 29.
19.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=6, Group=9.
20.	CLEAR SWITCH	Push to zero Panel=1 Row=6.
21.	PANEL 1 TOGGLE SWITCHES	Set switches 51-0 to the values recorded in step 6.
22.	LOAD SWITCH	Push to restore the original settings to Panel 1 Row 6.
23.	LOCAL BUFFER CONTROL	Restore the DSP switch to the DOWN position.
24.	SINGLE INST SWITCH	Restore to the OFF position.
25.	START SWITCH	Push to continue processing.

EU LOCAL STORAGE - ADDRESSING

The following addresses are used for accessing EU Local Storage:

WEW VALUE	RES BIT	REW VALUE	CONTENTS		
0	A	0	A/B	LOCATION 0	WORD 1
1	A	1	A/B	LOCATION 0	WORD 2 (D.P.)
2	A	2	A/B	LOCATION 1	WORD 1
3	A	3	A/B	LOCATION 1	WORD 2 (D.P.)

WEW VALUE	RES BIT	REW VALUE	CONTENTS		
4	B	0	B/A	LOCATION 0	WORD 1
5	B	1	B/A	LOCATION 0	WORD 2 (D.P.)
6	B	2	B/A	LOCATION 1	WORD 1
7	B	3	B/A	LOCATION 1	WORD 2 (D.P.)
8	R	0	R	LOCATION 0	
9	R	1	R	LOCATION 1	
A	R	2	R	LOCATION 2	
B	R	3	R	LOCATION 3	
C	W	0	W	LOCATION 0	
D	W	1	W	LOCATION 1	
E	W	2	W	LOCATION 2	
F	W	3	W	LOCATION 3	

EU LOCAL STORAGE READ

1. STATUS SWITCH — Place in the TEST position.

2. SINGLE INST SWITCH — Place in the ON position

3. PANEL 2 - ROW 1-21 DISPLAY SELECTION — Place in the DOWN position to display the "C" Register.

4. LOCAL BUFFER CONTROL — Place the LOC switch in the UP position.

NOTE

If the processor was running, please go to step 8.

5. SINGLE ROUTINE SWITCH — Place in the ON position.

6. START SWITCH — Push once to set up CPM for a EU Local Storage operation.

7. SINGLE ROUTINE SWITCH — Restore to the OFF position.

NOTE

End of special processing for a CPM that was not running.

8. LOCAL BUFFER CONTROL — Place the R/W switch in the UP position.

9. PANEL 2 ROW 1 — Record the setting of the "C" Register.

10.	THUMB WHEEEL SWITCHES	Set to Panel=2, Row-9, Group=9
11.	PANEL 2 ROW 9	Record the setting of all indicators in the row.
12.	CLEAR SWITCH	Push to zero Panel 2 Row 9.
13.	PANEL 2 TOGGLE SWITCHES	Set switches 50-45 to the appropriate values.
14.	LOAD SWITCH	Push to set RES and REW to the values specified in step 13.
15.	LOCAL BUFFER CONTROL	Toggle the PLS switch once, the output will appear in the "C" Register.
16.	CLEAR SWITCH	Push to zero Panel 2 Row 9
17.	PANEL 2 TOGGLE SWITCHES	Set to the values recorded in step 11.
18.	LOAD SWITCH	Push to restore the original contents of row 9.
19.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=1, Group=9.
20.	CLEAR SWITCH	Push to zero the "C" Register.
21.	PANEL 2 TOGGLE SWITCHES	Set to the values recorded in step 9.
22.	LOAD SWITCH	Push to restore the original contents of the "C" Register.
23.	LOCAL BUFFER CONTROL	Restore the R/W switch to the DOWN position.
24.	LOCAL BUFFER CONTROL	Restore the LOC switch to the DOWN position.
25.	SINGLE INST SWITCH	Restore to the OFF position.
26.	START SWITCH	Push to continue.

EU LOCAL STORAGE WRITE

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.

3.	PANEL 2 - ROW 1-21 DISPLAY SELECTION	Place in the DOWN position to display the "C" Register.
4.	LOCAL BUFFER CONTROL	Place the LOC switch in the UP position.

NOTE

If the processor was running, please go to step 8.

5.	SINGLE ROUTINE SWITCH	Place in the ON position.
6.	START SWITCH	Push once to set up CDM for local storage operation.
7.	SINGLE ROUTINE SWITCH	Restore to the OFF position.

NOTE

End of special processing for a processor that was not running.

8.	PANEL 2 ROW 1	Record the settings in the "C" Register.
9.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=9, Group=0.
10.	PANEL=2, ROW=9	Record the setting of the write counters and Write EU Storage.
11.	CLEAR SWITCH	Push to zero WEW.
12.	PANEL 2 TOGGLE SWITCHES	Set switches 3-0 to (the WEW hexidecimal value minus one).

NOTE

The address is incremented before the write occurs, therefore, the desired hexadecimal address minus one must be used to obtain the desired result, i.e.; To write in WEW="4" set WEW to "3"; To write in WEW="0" set WEW to "F".

13.	LOAD SWITCH	Push to set WEW to the values selected in step 12.
14.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=1, Group=9.

15.	PANEL 2 TOGGLE SWITCHES	Set switches 51-0 for the desired information.
16.	CLEAR SWITCH	Push to zero the "C" Register.
17.	LOAD SWITCH	Push to load the toggle switch settings in the "C" Register.
18.	LOCAL BUFFER CONTROL	Toggle the PLS switch once to write into EU Local Storage.

NOTE

To write the next word, repeat steps 15-18.

19.	CLEAR SWITCH	Push to zero the "C" Register.
20.	PANEL 2 TOGGLE SWITCHES	Set the values recorded in step 8.
21.	LOAD SWITCH	Push to restore the original contents of the "C" Register.
22.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=9, Group=0.
23.	CLEAR SWITCH	Push to zero WEW.
24.	PANEL 2 TOGGLE SWITCHES	Set switches 8-6, and 4-0 to the values recorded in step 10.
25.	LOAD SWITCH	Push to restore the original contents of the write counters and Write EU Storage.
26.	LOCAL BUFFER CONTROL	Restore the LOC switch to the DOWN position.
27.	SINGLE INST SWITCH	Restore to the OFF position.
28.	START SWITCH	Push to continue.

ASSOCIATIVE MEMORY READ

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.
3.	PANEL 2 ROW 1-21 DISPLAY SELECTION	Place in the UP position to display row 1.

4.	LOCAL BUFFER CONTROL	Place the ASM switch in the UP position.
5.	PANEL 2 ROW 1	Record the setting of all indicators in the row
6.	PANEL 2 ROW 4	Record the setting of DU (EWDV) in "EU Write Register Extras" (toggle switch position 40).
7.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=4, Group=9.
8.	PANEL 1 ROW 4	Record the setting of all indicators in the row.
9.	CLEAR SWITCH	Push to zero Panel 1 Row 4.
10.	PANEL 1 TOGGLE SWITCHES	Set switches 19-16 and switches 3-0 to the desired address (0-F hexadecimal).
11.	LOAD SWITCH	Push to load the specified address.
12.	LOCAL BUFFER CONTROL	Place the R/W switch in the UP position. The output should immediately appear in EWR.

NOTE

For sequential reads of Associative Memory, toggle the PLS switch under Local Buffer Control. This will cause the address to count and the next word to be accessed.

13.	LOCAL BUFFER CONTROL	Restore the R/W switch to the DOWN position.
14.	CLEAR SWITCH	Push to zero Panel 1 Row 4.
15.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in step 8.
16.	LOAD SWITCH	Push to restore the original contents of Panel 1 Row 4.
17.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=1, Group=9.
18.	CLEAR SWITCH	Push to zero the EW Register.
19.	PANEL 2 TOGGLE SWITCHES	Set to the values recorded in step 5.
20.	LOAD SWITCH	Push to restore the original contents of the EW Register.

NOTE

If the EW Data Valid bit currently has the same value as that obtained in step 6 please go to step 28.

NOTE

If EWDV is presently not set perform steps 21, 22, and 23.

NOTE

If EWDV is presently set, perform steps 21, and 24-27.

21.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=4, Group=4.
22.	PANEL 2 TOGGLE SWITCHES	Set switch 40, all other switches must be reset (down).
23.	LOAD SWITCH	Push to set EWDV.
24.	PANEL 2 ROW 4	Record the settings of ME49-45, NT, NC, NV, and PV.
25.	CLEAR SWITCH	Push to zero EWDV.
26.	PANEL 2 TOGGLE SWITCHES	Set switches 49-41 to the values recorded in step 24. Switch 40 must be down (FALSE).
27.	LOAD SWITCH	Push to restore the original contents of ME49-45, NTt NCt NVt PV, and DV.

NOTE

End of special EWR Data Valid processing.

28.	LOCAL BUFFER CONTROL	Restore the ASM switch to the DOWN position.
29.	SINGLE INST SWITCH	Restore to the OFF position.
30.	START SWITCH	Push to continue.

ASSOCIATIVE MEMORY WRITE

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.
3.	PANEL 1 ROW 1-21 DISPLAY SELECTION	Place in the DOWN position to display the Input Register.

4.	LOCAL BUFFER CONTROL	Place the ASM switch in the UP position.
5.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=4, Group=9.
6.	PANEL 1 ROW 4	Record the setting of all indicators in the row.
7.	CLEAR SWITCH	Push to zero the row.
8.	PANEL 1 TOGGLE SWITCHES	Set switches 19-16 and switches 3-0 to the desired address (0-F hexadecimal).
9.	LOAD SWITCH	Push to load the specified address.
10.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=1, Group=9.
11.	Panel 1 Row 1	Record the setting of all indicators in the row.
12.	CLEAR SWITCH	Push to zero the Input Register.
13.	PANEL 1 TOGGLE SWITCHES	Set 51-0 for the information to be placed in Associative Memory. Parity (odd) must be maintained.
14.	LOAD SWITCH	Push to load the toggle switch settings in the Input Register.
15.	LOCAL BUFFER CONTROL	Toggle the PLS switch once to write to Associative Memory.

NOTE

For additional sequential writes please repeat steps 12-15.

16.	CLEAR SWITCH	Push to zero the Input Register.
17.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in step 11.
18.	LOAD SWITCH	Push to restore the original setting of the Input Register.
19.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=4, Group=9.
20.	CLEAR SWITCH	Push to zero row 4.

21.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in step 6.
22.	LOAD SWITCH	Push to restore the original contents of row 4.
23.	LOCAL BUFFER CONTROL	Restore the ASM switch to the DOWN position.
24.	SINGLE INST SWITCH	Restore to the OFF position.
25.	START	Push to continue.

ASSOCIATIVE ADDRESS MEMORY READ

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position
3.	PANEL 2 ROW 1-21 DISPLAY SELECTION	Place in the UP position to display row 1.
4.	LOCAL BUFFER CONTROL	Place the ASM switch in the UP position.
5.	LOCAL BUFFER CONTROL	Place the ASA switch in the UP position.
6.	PANEL 2 ROW 1	Record the setting of all indicators in the row.
7.	PANEL 2 ROW 4	Record the setting of DV (EWDV) in "EU Write Register Extras (toggle switch position 40).
8.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=4, Group=9.
9.	PANEL 1 ROW 4	Record the setting of all indicators in the row.
10.	CLEAR SWITCH	Push to zero Panel 1 Row 4.
11.	PANEL 1 TOGGLE SWITCHES	Set switches 19-16 and switches 3-0 to the desired address (0-F hexadecimal).
12.	LOAD SWITCH	Push to load the specified address.
13.	LOCAL BUFFER CONTROL	Place the R/W switch in the UP position. The output should immediately appear in EWR.

NOTE

The format of the addresses which appear in EWR is as follows:

BITS	CONTENTS
51,50	Not used.
49-39	1st part of even address
38,37	Not used
36-26	2nd part of even address
25,24	Not used
23-13	1st part of odd address
12,11	Not used
10-0	2nd part of odd address

NOTE

For sequential reads of Associative Address Memory, Toggle the PLS switch under Local Buffer Control. This will cause the address to count and the next word to be accessed.

14. LOCAL BUFFER CONTROL — Restore the R/W switch to the DOWN position.

15. CLEAR SWITCH — Push to zero Panel 1 Row 4.

16. PANEL 1 TOGGLE SWITCHES — Set switches 51-0 to the values recorded in step 9.

17. LOAD SWITCH — Push to restore the original contents of Panel 1 Row 4.

18. THUMB WHEEL SWITCHES — Set to Panel=2, Row-1, Group=9.

19. CLEAR SWITCH — Push to zero EWZ.

20. PANEL 2 TOGGLE SWITCHES — Set switches 51-0 to the values recorded in step 6.

21. LOAD SWITCH — Push to restore the original contents of EWR.

NOTE

If the EW Data Valid bit currently has the same value as that obtained in step 7 please go to step 29.

NOTE

If EWDV is presently not set perform steps 22-24.

NOTE

If EWDV is presently set, perform steps 22, 25-28.

22.	THUMB WHEEL SWITCHES	Set to Panel=2, Row=4, Group-4.
23.	PANEL 2 TOGGLE SWITCHES	Set switch 40, all other switches must be down (RESET).
24.	LOAD SWITCH	Push to set EWDV.
25.	PANEL 2 ROW 4	Record the setting of ME49-45, NT, NC, NV, and PV.
26.	CLEAR SWITCH	Push to zero EWDV.
27.	PANEL 2 TOGGLE SWITCHES	Set switches 49-41 to the values recorded in step(25. Switch 48 must be down (False).
28.	LOAD SWITCH	Push to restore the original contents of ME49-45, NT, NC, NV, PV, and DV.

NOTE

End of special EWR Data Valid processing.

29.	LOCAL BUFFER CONTROL	Restore the ASA switch to the DOWN position.
30.	LOCAL BUFFER CONTROL	Restore the ASM switch to the DOWN position.
31.	SINGLE INST SWITCH	Restore to the OFF position.
32.	START SWITCH	Push to continue processing.

ASSOCIATIVE ADDRESS MEMORY WRITE

1.	STATUS SWITCH	Place in the TEST position.
2.	SINGLE INST SWITCH	Place in the ON position.
3.	LOCAL BUFFER CONTROL	Place the ASM switch in the UP position.
4.	LOCAL BUFFER CONTROL	Place the ASA switch in the UP position.

NOTE

The control clear switch clears the associative address memory. Turning on the ASM DISABLE switch will inhibit this clearing action.

5.	THUMB WHEEL SWITCHES	Set to Panel=1, Row-4, Group=9.
6.	PANEL 1 ROW 4	Record the setting of all indicators in the row.
7.	CLEAR SWITCH	Push to zero Panel 1 Row 4.
8.	PANEL 1 TOGGLE SWITCHES	Set switches 19-16 and switches 3-0 to the desired address (0-F hexadecimal).
9.	LOAD SWITCH	Push to load the specified address.
10.	THUMB WHEEL SWITCHES	Set to Panel=1, Row-2, Group=9.
11.	PANEL 1 ROW 2	Record the setting of all indicators in the row.
12.	CLEAR SWITCH	Push to zero Panel 1 Row 2.
13.	PANEL 1 TOGGLE SWITCHES	Set switches 19-0 to the desired main memory address and switches 21-20 to the residue for that address.
14.	LOAD SWITCH	Push to load the toggle switch settings in the Comm Address.
15.	LOCAL BUFFER CONTROL	Toggle the PLS switch once to write to Associative Address Memory.

NOTE

To write to sequential Associative Address Memory addresses, please repeat steps 12-15.

16.	CLEAR SWITCH	Push to zero Panel 1 Row 2.
17.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in step 11.
18.	LOAD SWITCH	Push to restore the original contents of Panel 1 Row 2.
19.	THUMB WHEEL SWITCHES	Set to Panel=1, Row=4, Group=9.
20.	CLEAR SWITCH	Push to zero Panel 1 Row 4.
21.	PANEL 1 TOGGLE SWITCHES	Set to the values recorded in step 6.

22.	LOAD SWITCH	Push to restore the original contents of Panel 1 Row 4.
23.	LOCAL BUFFER CONTROL	Restore the ASA switch to the DOWN position.
24.	LOCAL BUFFER CONTROL	Restore the ASM switch to the DOWN position.
25.	SINGLE INST SWITCH	Restore to the OFF position.
26.	START	Push to continue.

SECTION 3
INPUT/OUTPUT MODULE PANELS

This section presents an overall view of the input/output module (IOM) in figure VII-3-1 and close-up views of the panels of the input/output module in figures VII-3-2 and VII-3-3.

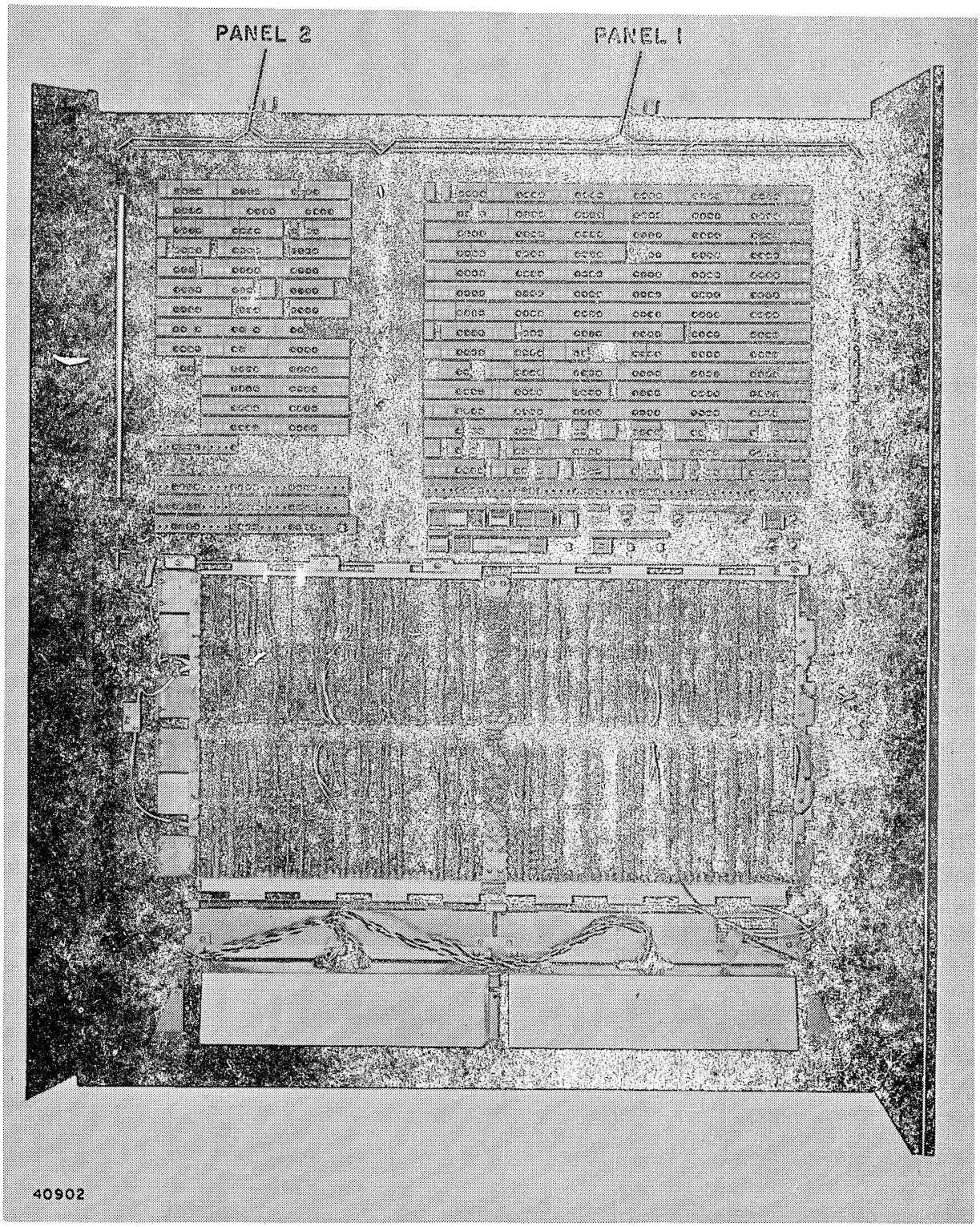
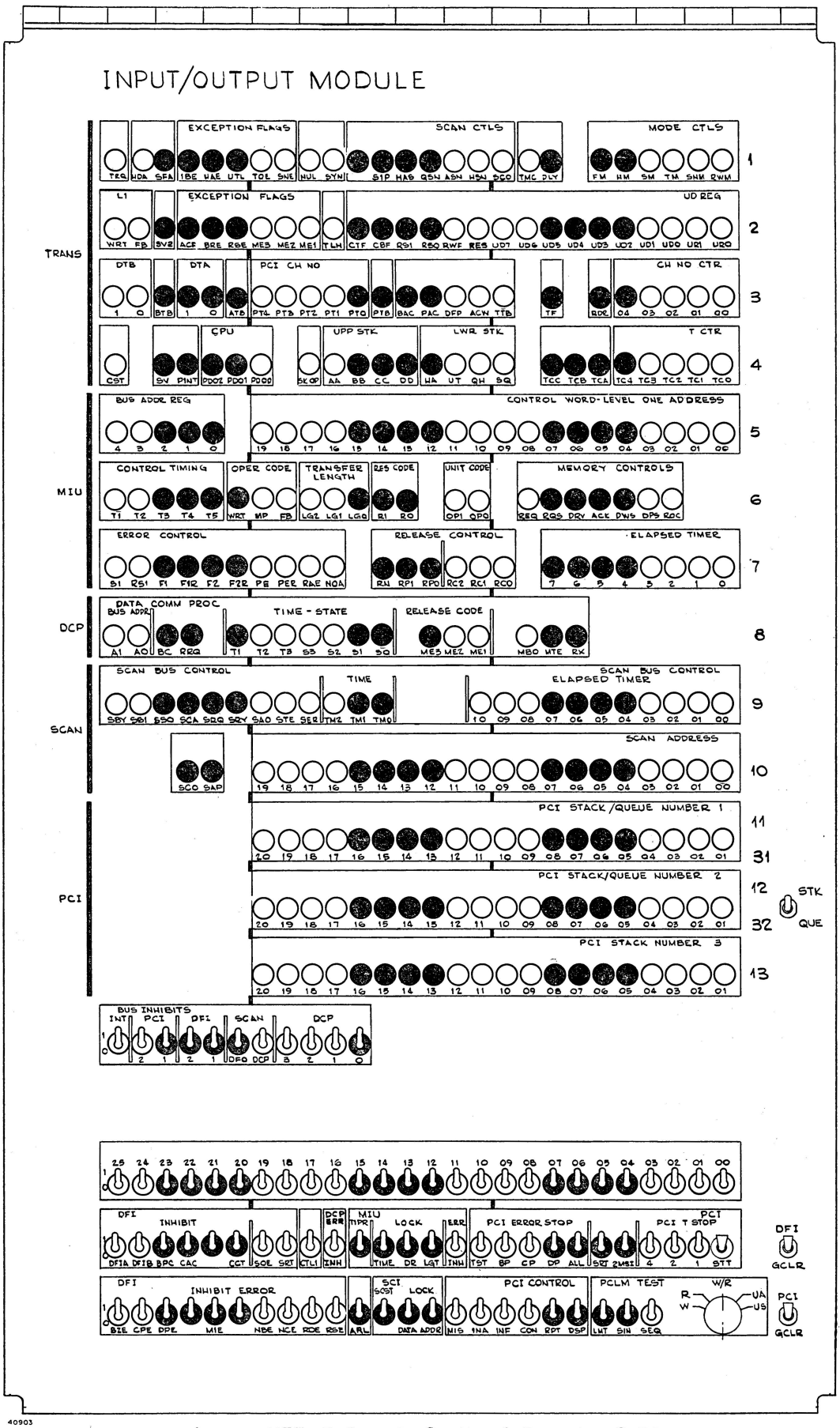


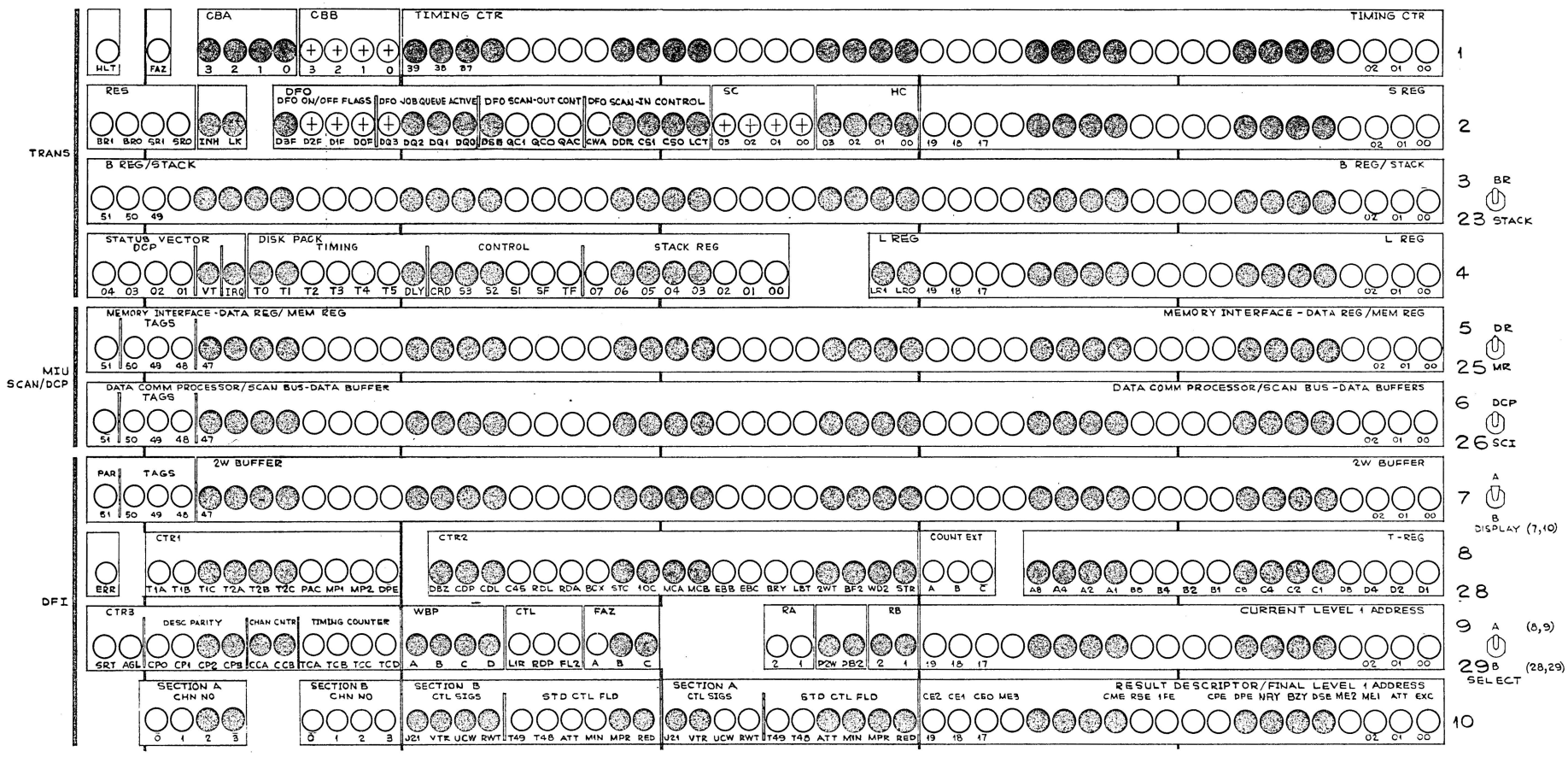
Figure VII-3-1. Overall View of IOM



40903

Figure VII-3-2. Left-Hand Panel of IOM

INPUT/OUTPUT MODULE



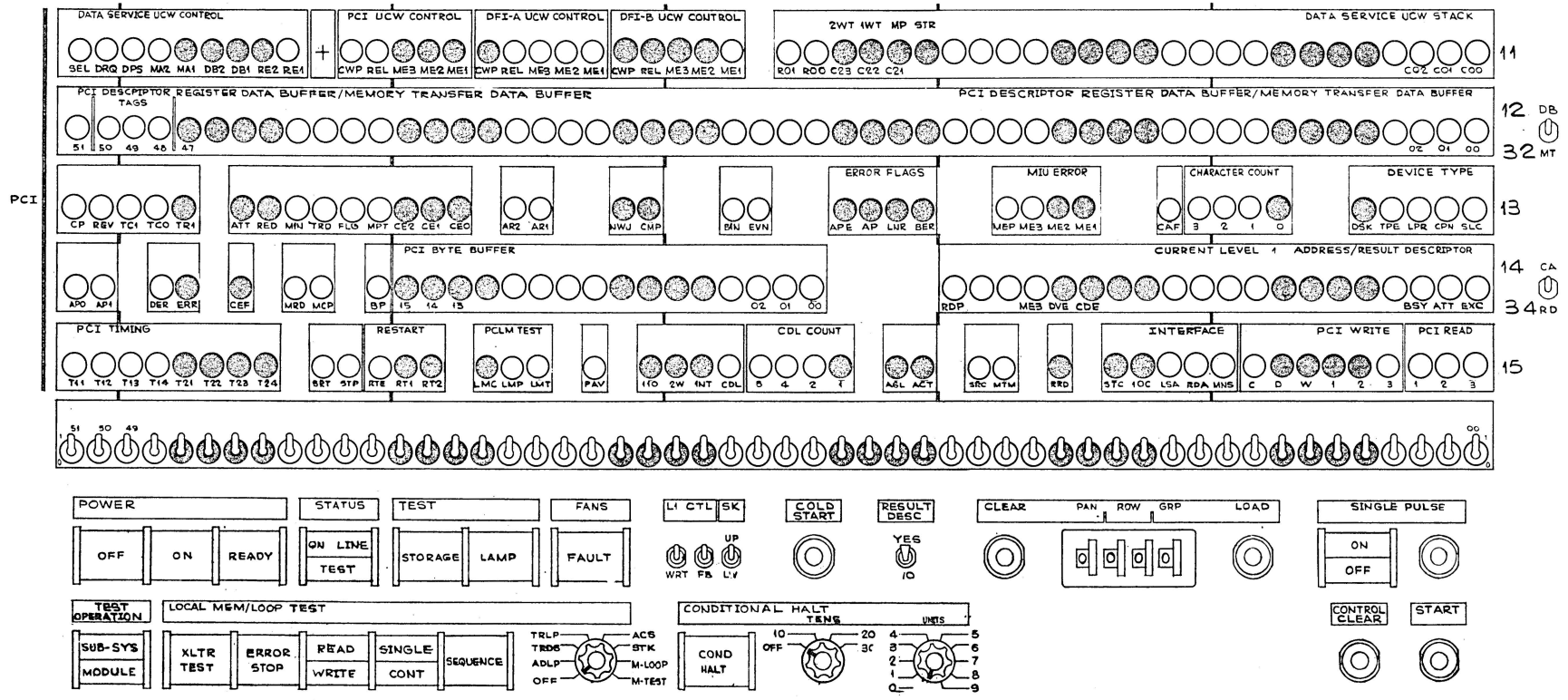


Figure VII-3-3. Right-Hand Panel of IOM

SECTION 4
MEMORY CONTROL MODULE PANEL

This section describes the functions and uses of the controls and indicators on the panel of the memory control module (MCM). An overall view of the memory control module is shown in figure VII-4-1, and a close-up of the panel is shown in figure VII-4-2.

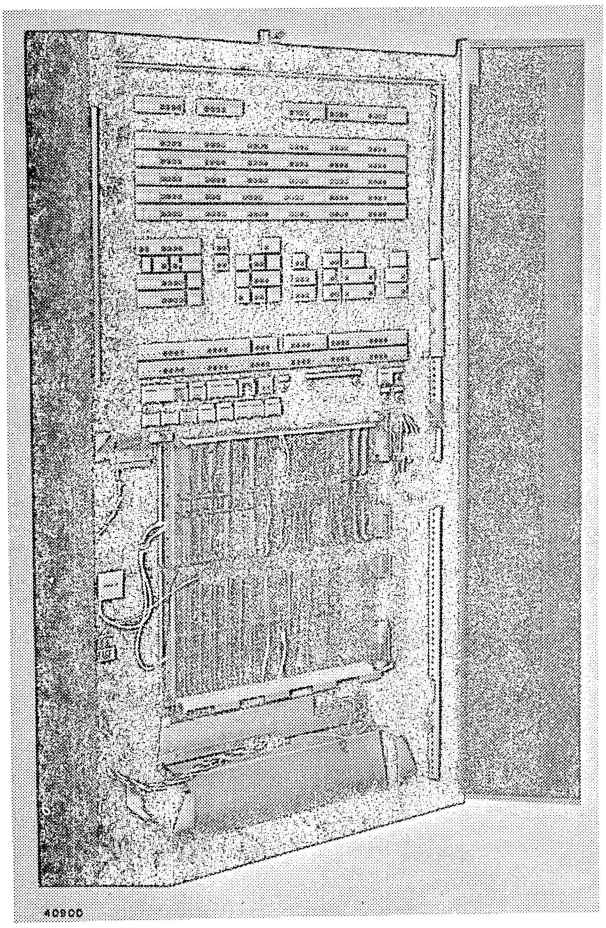


Figure VII-4-1. Overall View of MCM

ROWS 1 THROUGH 12

Row 1

REQUESTOR - Stores request signals from requestors for evaluation by the priority resolver.

COM FAILURE INHIBITS - Used to prevent a requestor from locking up the priority resolver if he has sent a request without a request strobe or to prevent a requestor from obtaining consecutive services if a lower priority requestor is waiting.

REQUESTOR INHIBIT REG - Used to lock out certain requestors from access to this

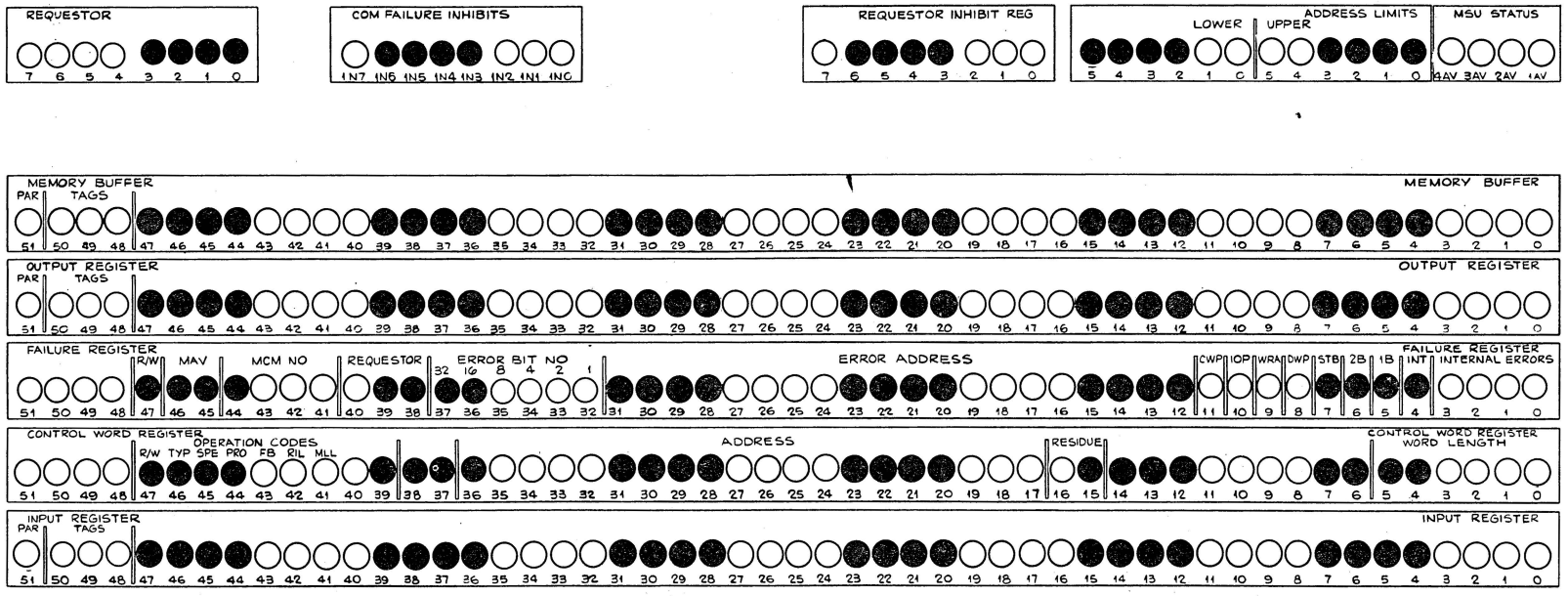
ADDRESS LIMITS

LOWER - Contains the most significant six bits of the lowest memory address available to the MCM. Can be programmatically loaded by a CPM.

UPPER - Contains the most significant six bits of the highest memory address available to the MCM. Can be programmatically loaded by a CPM.

MSU STATUS - Indicates which of the four possible MSU's are available to the MCM. Can be programmatically loaded by a CPM.

MEMORY CONTROL MODULE



4090A

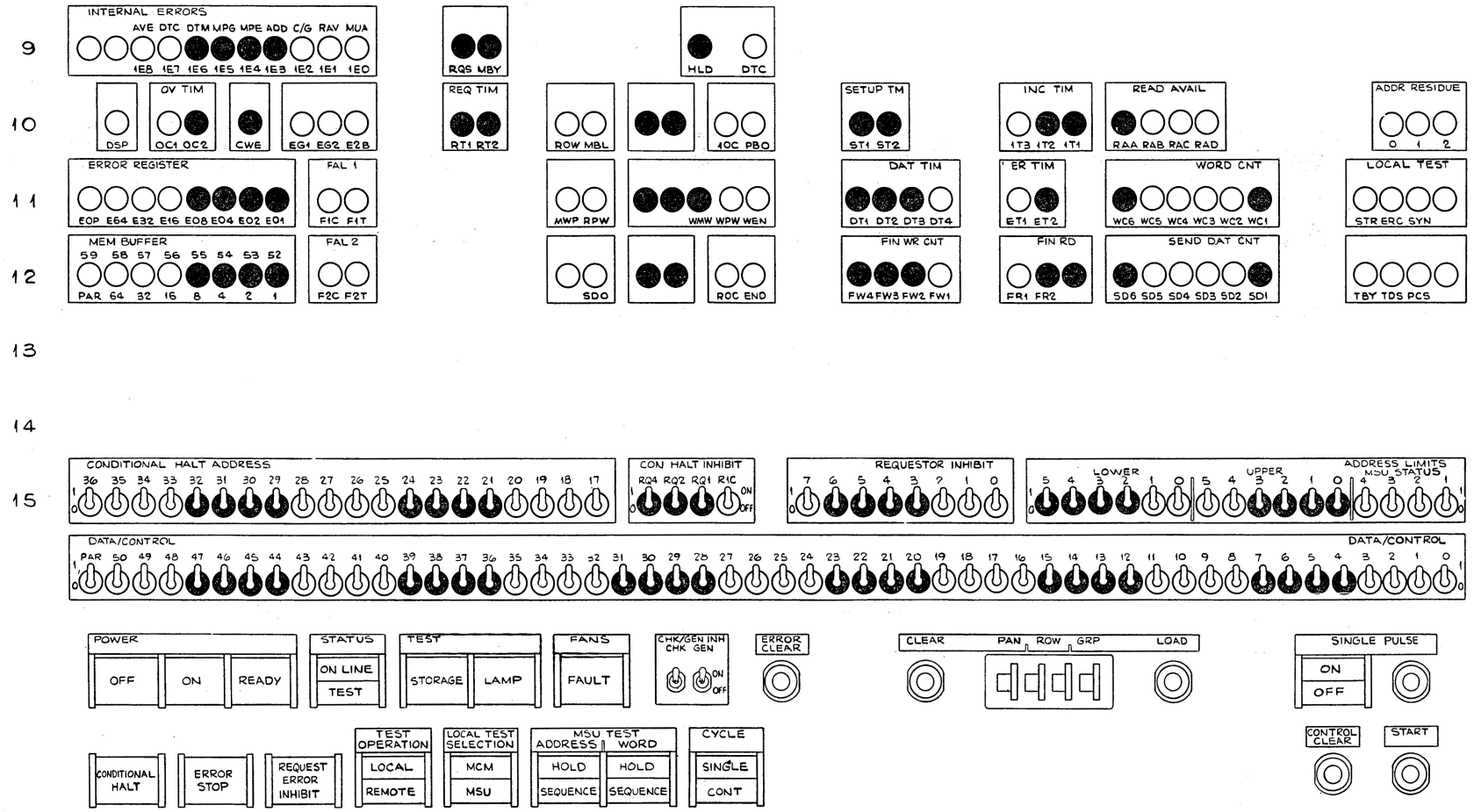


Figure VII-4-2. Panel of MCM

Row 3

MEMORY BUFFER - The Memory Buffer Register is a 60-bit buffer register for data transferred to or from the MSU's. Bits 52-59, the error-code check bits and overall parity bit, are displayed in Row 12 of the panel.

Row 4

OUTPUT REGISTER - The Output Register is used to buffer data words that are being transmitted to a requestor.

Row 5

FAILURE REGISTER - The Failure Register is used to contain all pertinent information necessary to identify and define a failure.

Row 6

CONTROL WORD REGISTER - The Control Word Register is used to contain the control words transmitted by the requestor.

Row 7

INPUT REGISTER - The Input Register is used to temporarily buffer words received from a requestor.

Row 9

INTERNAL ERRORS - Internal Errors Register, used to record internal errors detected by the MCM. The errors detected are:

AVE - MSU Availability Error

DTC - Data Transfer Control (DTC) failure

DTM - Data Timer failure

MPG - Parity Generator (MSU Control) failure

MPE - MSU Parity Error

ADD - Address Counter failure

C/G - Checker/Generator failure

RAV - Read Available failure

MUA - MSU Unavailable

RQS - Special Request flip-flop, indicates that a CPM is making a special request in order to load memory limits or requestor inhibits, or to fetch the fail register. This type of operation bypasses the requestor inhibits.

MBY - MCM Busy flip-flop, used to inhibit access by other requestors until all communications for the using requestor are complete.

HLD - Hold flip-flop, used to allow lockup of the MCM whenever the error stop option is in effect and certain error conditions occur, or during conditional halt operations.

DTC - Data Transfer Control, used for transfer of controls and data within the MCM.

Row 10

DSP - Data Strobe Problem flip-flop, used to indicate when too many or too few strobes have been sent by requestor.

OV TIM (OC1, OC2) - Overflow Clear Timer, controls the timing for

clear/release of MCM from operation requested, due to some lockup type of failure in the requested operation.

CWE - Control Word Error flip-flop, indicates that any of the following errors was detected in the control word:

1. Parity.
2. Wrong MCM Address.
3. Illegal Operation.

EG1 - Indicates that the group 1 area of the Fail Register is locked with fail information.

EG2 - Indicates that the group 2 area of the Fail Register is locked with fail information.

E2B - Indicates an even number of bits in error in the word received from an MSU.

REQ TIM (RT1, RT2) - Requestor Timer, used in priority resolution. It is initiated each time a new request is made to the MCM.

ROW - Read Or Write flip-flop, used as a basic control during either a read or write operation. Set for a read operation and for the read portion of a protected write or flashback operation. Reset for a write operation.

MBL - Memory Buffer Load flip-flop, indicates that the memory buffer register is loaded, and is used to generate other controls as required by the operation being performed.

IOC - Input/Output Control flip-flop, used to control the direction of data transfer between MCM and requestor. Set during read operation or read portion of a protected write or flashback operation. Reset during a write operation.

PBO - Presence Bit On flip-flop, indicates that the output register is loaded with data during a read operation.

SETUP TIM (ST1, ST2) - Set-up Timer, used to control initialization of any operation within the MCM.

INC TIM (IT3, IT2, IT1) - Timing counter used to prevent lock-up of MCM for such failures as no read available signal from MSU or no data strobe from requestor in N word write type operations.

READ AVAIL (RAA, RAB, RAC, RAD) - Read Available register, used to store the read available signal transmitted from the selected MSU.

ADDR RESIDUE - Address Residue Counter, used to generate a residue from the address field of a control word. This residue is then compared to the residue field of the control word to detect any error which may have occurred during the transfer.

Row 11

ERROR REGISTER - Indicates errors detected by the error detection and correction logic. Each bit indicates an error in its respective error correction group.

FAL 1 (F1C, F1T) - Controls the transmission and duration of the FAIL 1 (irrecoverable failure) signal to the requestor.

MWP - Memory Word Protected flip-flop, indicates if a memory word is protected (bit 48 set) during the read portion of a protected write operation.

RPW - Remember Protected Word flip-flop, used to maintain a record that a protected word, 2-bit error, or memory parity error was encountered during a protected write operation.

WMW - Write Multi-Word flip-flop, indicates that timing control of a N-length operation is under control of the requestor data strobe.

WPW - Write Protected Word flip-flop, used to control the writing of a protected word back into its original location on a protected write operation.

WEN - Write Enable flip-flop, used to control writing of data words into the MSU's.

DATA TIM (DT1-DT4) - Data Timer, used to control which MSU is selected during an operation.

ER TIM (ET1, ET2) - Error Timer, used to control single-bit error correction, failure recording, and initiation of failure reporting.

WORD CNT (WC6-WC1) - Word Counter, used to monitor the number of words transferred during any N length operation.

LOCAL TEST

STR - Enables start of any local test operation from the START push button on the MCM panel.

ERC - Allows clear of Fail Register and reset of hold condition in error stop mode of operation.

SYN - Synchronizes start of any local test operation or error clear operation with the 8 MHZ clock.

Row 12

MEM BUFFER - Memory Buffer Register, used to buffer data transferred to or from the MSU's. This portion of the register contains the check bits and overall parity bit. Bits 0-51 are displayed on Row 3 of the panel.

FAL 2 (F2C, F2T) - Controls the transmission and duration of the FAIL 2 (recoverable failure) signal to the requestor.

SDO - Send Data On flip-flop, used to control the down counting of the Send Data Counter.

ROC - Requestor Operation Complete flip-flop, used to control the sending of the Requestor Operation Complete signal to the requestor.

END - Indicates the end of any operation within the MCM that does not require final read timing.

FIN WR CNT (FW4-FW1) - Final Write Timer, used to control completion of any write operation.

FIN RD (FR1, FR2) - Final Read Timer, used to time out the final portion of a read operation.

SEND DATA CNT (SD6-SD1) - Send Data Counter, used to control the number of words requested from the requestor during a N-length write operation. It is down counted as each data word is sent from the requestor.

It is loaded from the word length field of the control word, limited by the number of MSU's available, or limited to one if the address is less than eight words from the end of an MSU.

TBY - Test Busy signal, acts as local requestor flip-flop for local test operation of MCM.

TDS - Test Data Strobe flip-flop, provides data strobe for local test operation of MCM.

PCS - Generates a non-ringing CLEAR signal for the MSU's from a push-button source at the operator's console.

SWITCHES AND INDICATORS

CONDITIONAL HALT ADDRESS SWITCHES - Select program address to be monitored during any writes into memory.

CONDITIONAL HALT INHIBIT SWITCHES

REQUESTOR INHIBIT CONTROL (RIC)

OFF POSITION - In conditional halt operation lock up of MCM will occur whenever monitored program address is written into.

ON POSITION - Selected requestor is allowed to override conditional halt operation.

REQUESTOR NUMBER SWITCHES (RQ4, RQ2, RQ1) - Select requestor who is allowed to override conditional halt operation.

REQUESTOR INHIBIT SWITCHES - Sets or resets respective FF's each time:

1. Power is cycled up in MCM.

2. CONTROL CLEAR push button is depressed in local test of MCM.

3. CLEAR is depressed on operator's console.

ADDRESS LIMITS SWITCHES (Lower, Upper, and MSU Status) - Same as for requestor inhibit switches.

DATA/CONTROL SWITCHES - Settings used for control word or write data word for local test of MCM.

POWER ON SWITCH - Applies power to MCM and MSU's if in remote.

POWER OFF SWITCH - Removes power from MCM and MSU's if in remote.

POWER READY INDICATOR - Lights at completion of power-on sequence.

STATUS SWITCH

ON LINE POSITION - MCM is in on line operation. All test controls disabled.

TEST POSITION - MCM is in test operation. All test controls may be activated.

TEST

LAMP SWITCH - Enables lamp test of indicators selected by the group thumb-wheel switch.

STORAGE SWITCH - Enables set of all rows equal to pattern set in data/control switches.

FANS FAULT INDICATOR - Illuminates if failure of a cooling fan is detected. If this occurs, the MCM is powered off.

CHECKER INHIBIT SWITCH - Inhibits detection of 1-or 2-bit errors when on.

GENERATOR INHIBIT SWITCH - Inhibits changing of check bits and overall parity bit loaded into memory buffer during write operations.

ERROR CLEAR - Resets the following when depressed:

1. Failure Register.
2. Error Group 1 (EG1) FF.
3. Error Group 2 (EG2) FF.
4. Hold (HLD) FF.

PANEL/ROW/GROUP THUMBWHEELS

PANEL - Selects panel (set to position 1 for MCM).

ROW - Selects register for loading from data/control switches.

GROUP - Selects group for loading from data/control switches or to test in lamp test.

CLEAR PUSH BUTTON - Clears FF's selected by PANEL/ROW/GROUP thumbwheels.

LOAD PUSH BUTTON - Load FF's selected by PANEL/ROW/GROUP thumbwheels.

SINGLE PULSE SWITCH

ON POSITION - 8 MHZ clock disabled within MCM.

OFF POSITION - 8 MHZ clock enabled within MCM.

SINGLE PULSE PUSH BUTTON - Generates clock pulse each time push button is depressed with SINGLE PULSE switch on.

CONDITIONAL HALT SWITCH - Enables conditional halt operation for writes into memory.

ERROR STOP SWITCH - Enables lock up of MCM for any FAIL1, FAIL2 conditions detected (exception - any detection disabled by requestor error inhibit switch or by CHECKER INHIBIT on/off switch).

REQUESTOR ERROR INHIBIT SWITCH - Disables detection of following errors:

1. Control Word Parity.
2. Wrong MCM Address.
3. Write Data Word Parity Error.
4. Data Strobe Error.

TEST OPERATION SWITCH

LOCAL POSITION - Enables local testing of the MCM (requestors not needed for testing).

REMOTE POSITION - Enables remote testing of the MCM (requestor/requestors needed for testing).

LOCAL TEST SELECTION

MCM POSITION - Enables logic oriented towards testing of the MCM.

MSU POSITION - Enables logic oriented towards testing of MSU's.

MSU TEST SWITCHES

ADDRESS HOLD, WORD HOLD - Single address will be tested within memory.

ADDRESS HOLD, WORD SEQUENCE - Allows word to sequence while address is held (NOTE - this operation should not be used with single MSU).

ADDRESS SEQUENCE, WORD HOLD - Allows test to be executed sequentially on each address within an MSU.

ADDRESS SEQUENCE, WORD SEQUENCE - Allows test to be executed sequentially on each address within the memory available to the MCM.

CYCLE SWITCH

SINGLE POSITION - Only one cycle of test will be executed each time the START push button is depressed.

CONTINUOUS POSITION - Test will be executed continuously.

NOTE

Termination of continuous cycle testing should be accomplished by placing the CYCLE switch in the SINGLE position. It should never be terminated through use of the CONTROL CLEAR push button.

CONTROL CLEAR PUSH BUTTON - Resets the following when pressed:

1. All controls.
2. Control Word Register.
3. Failure Register.

Loads the requestor inhibit and memory limits registers from their respective switches when depressed.

START PUSH BUTTON - Used to initiate any local test of the MCM.

MCM PANEL OPERATIONS

In order to enable the remaining panel controls the STATUS switch must be in the TEST position. The panel thumbwheel must be in Position 1, since the MCM has only one panel.

Lamp Test

Turn the LAMP TEST switch on, and place all DATA/CONTROL switches in the 1 position. Set the GROUP thumbwheel to the 0 position and depress the LOAD push button. Flip-flops 0-9 of all rows will light. Stepping the GROUP thumbwheel from positions 0 thru 5 and depressing the LOAD push button at each position will cause the indicators in all rows to light in groups of 10.

Storage Test

Turn on the SINGLE PULSE and STORAGE TEST switches, and place all DATA/CONTROL switches in the 1 position. Press the CLEAR push button, and all indicators should be out. Press the LOAD push button and all indicators light except for spare indicators.

Register Loading

Place the TEST OPERATION switch in LOCAL. Place the ROW thumbwheel in the position corresponding to the row number of the register to be loaded. Place the GROUP thumbwheel in position 9. Set the desired bit configuration into the DATA/CONTROL switches. Press the CLEAR push button to clear the original contents

of the register. Press the LOAD push button, and the contents of the DATA/CONTROL switches are loaded into the selected register.

Single Word Operations (Read or Write)

Position the following switches as indicated:

STATUS Switch - TEST position

CHECKER INHIBIT Switch - OFF

GENERATOR INHIBIT Switch - OFF

CONDITIONAL HALT Switch - OFF

ERROR STOP Switch - ON

**REQUESTOR ERROR INHIBIT Switch- OFF

TEST OPERATION Switch - LOCAL position

LOCAL TEST SELECTION Switch - MSU position

*ADDRESS SEQUENCE/HOLD Switch - HOLD position

*WORD SEQUENCE/HOLD Switch - HOLD position

**CYCLE Switch - SINGLE position

SINGLE PULSE Switch - OFF

Load the Control Word Register with a control word indicating the desired operation. The ADDRESS field should contain the desired memory address and the WORD LENGTH field should equal 1. The OPERATION CODE field should be set as follows:

OPERATION	BIT 47	46	45	44	43
Single Word Overwrite	1	0	1	0	0
Single Word Overwrite with Flashback	1	0	1	0	1
Single Word Fetch	0	0	1	0	0
Single Word Protected Write	1	0	1	1	0

All remaining bits in the control word should be zero.

For any variation of write, load the Input Register with the data word to be written. The parity bit should be set correctly for this word.

Press the START push button. The operation will take place.

*If the ADDRESS and WORD SEQUENCE/HOLD switches are set to the SEQUENCE position, the indicated operation will be repeated for consecutive memory addresses each time the START push button is pressed.

**If the ADDRESS and WORD SEQUENCE/HOLD switches are set to the SEQUENCE position and the CYCLE switch is set to the CONT position, the indicated operation will be repeated for all consecutive address to the limit of the available memory or until an error is detected. If the REQUESTOR ERROR INHIBIT switch is turned OFF, the operation will repeatedly cycle through memory until an error is detected.

Conditional Halt Operation

The CONDITIONAL HALT switch should be turned on, the ERROR STOP and REQUEST ERROR INHIBIT switches should be off, and the TEST OPERATION

switch should be in the REMOTE position. The CONDITIONAL HALT ADDRESS switches should be set to the memory address which is to be monitored for write operations. The CONDITIONAL HALT INHIBIT switches may be used to allow one requestor to override the conditional halt operation.

SECTION 5
MAINTENANCE DIAGNOSTIC UNIT PANELS

This section presents an overall view of the maintenance diagnostic unit in figure VII-5-1, and close-up views of the panels of the MDU in figures VII-5-2, VII-5-3, and VII-5-4.

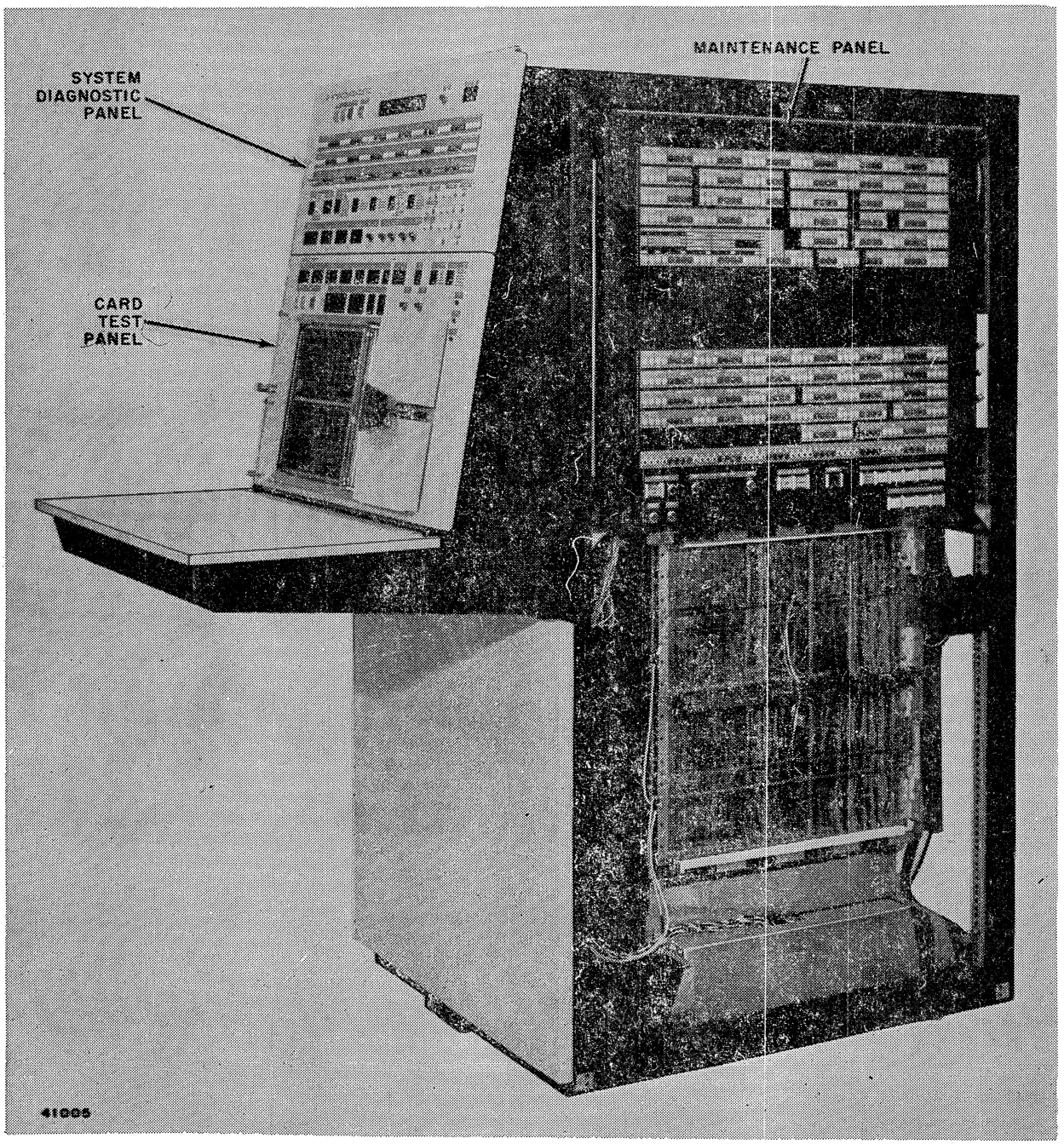


Figure VII-5-1. Maintenance Diagnostic Unit

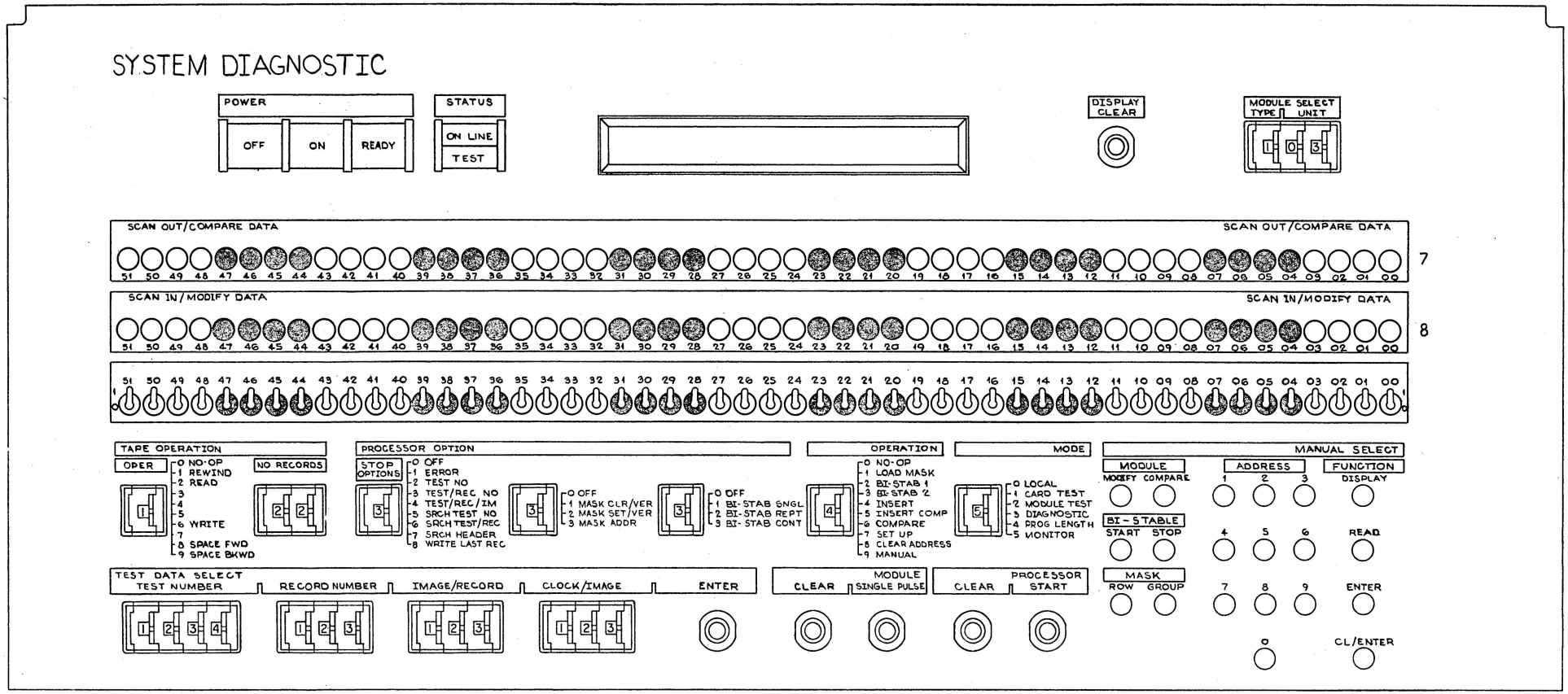


Figure VII-5-2. System Diagnostic Panel

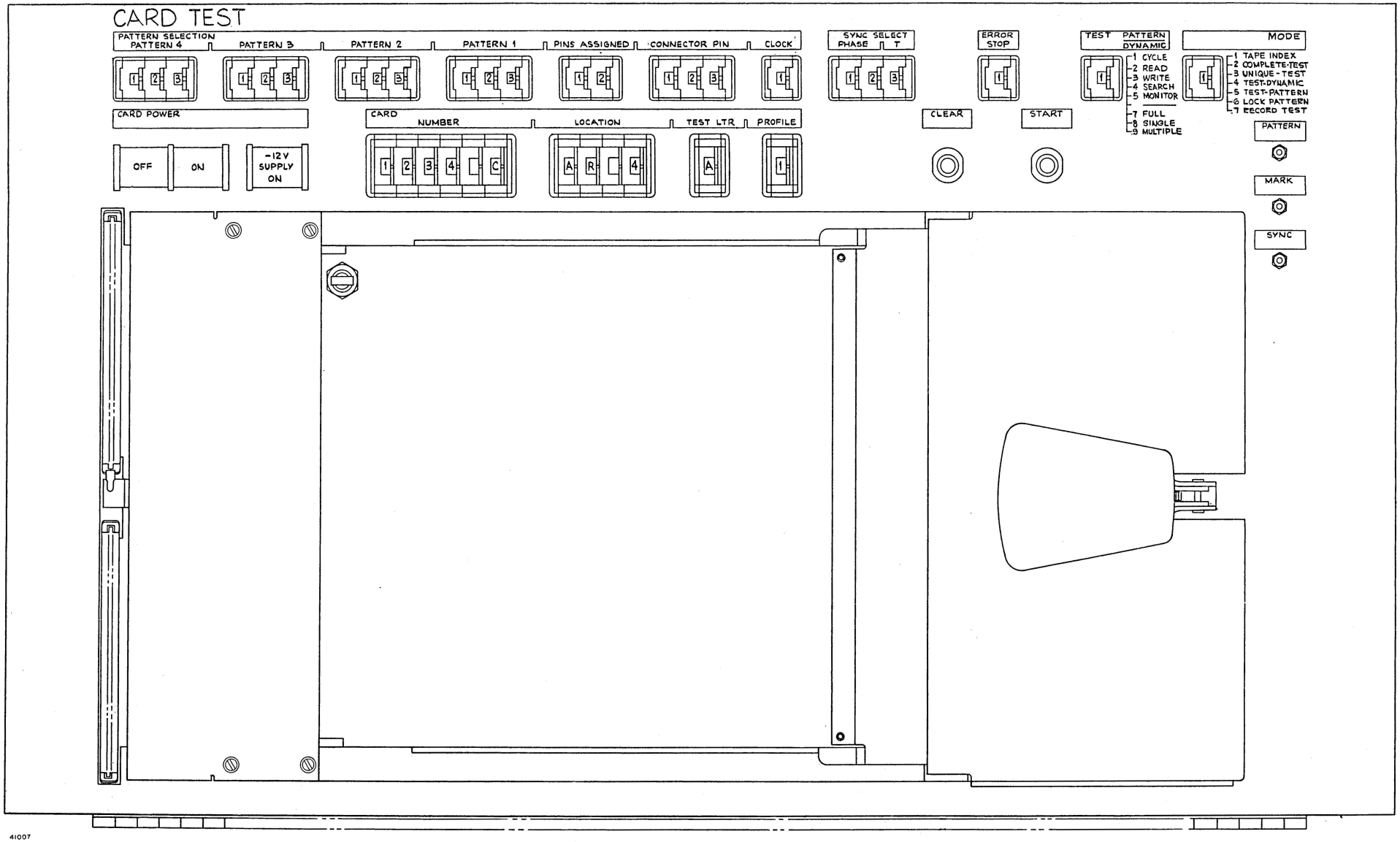
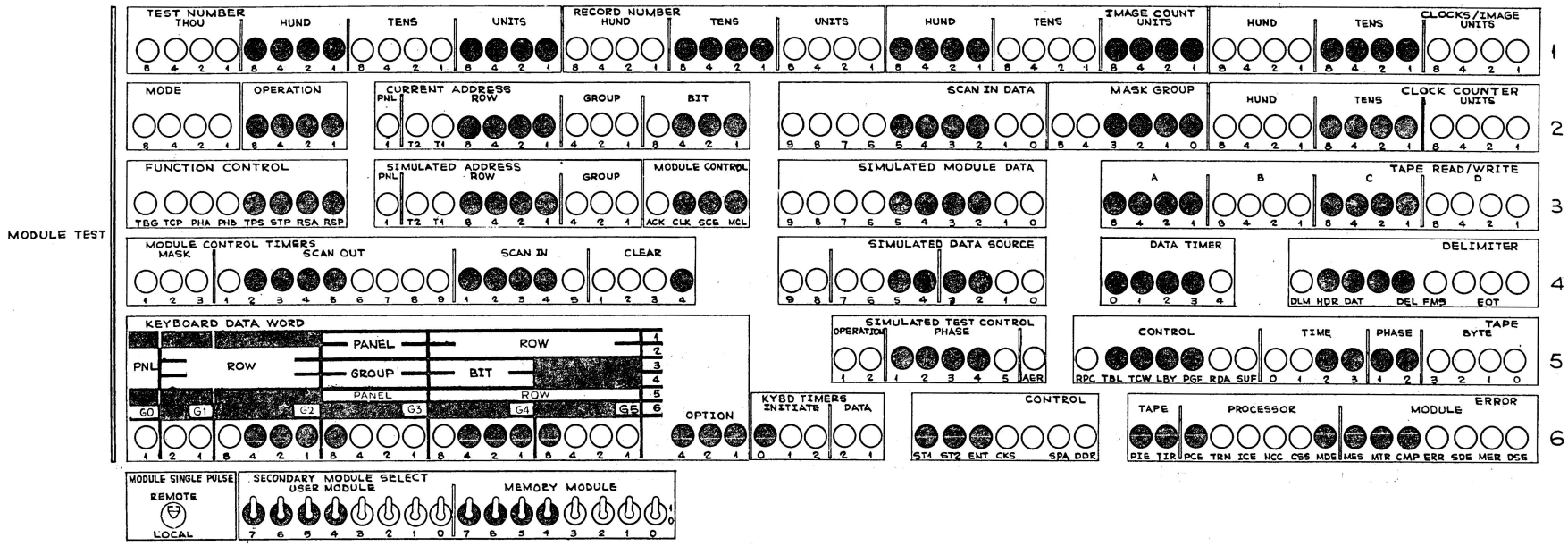


Figure VII-5-3. Card Test Panel

MAINTENANCE DIAGNOSTIC UNIT



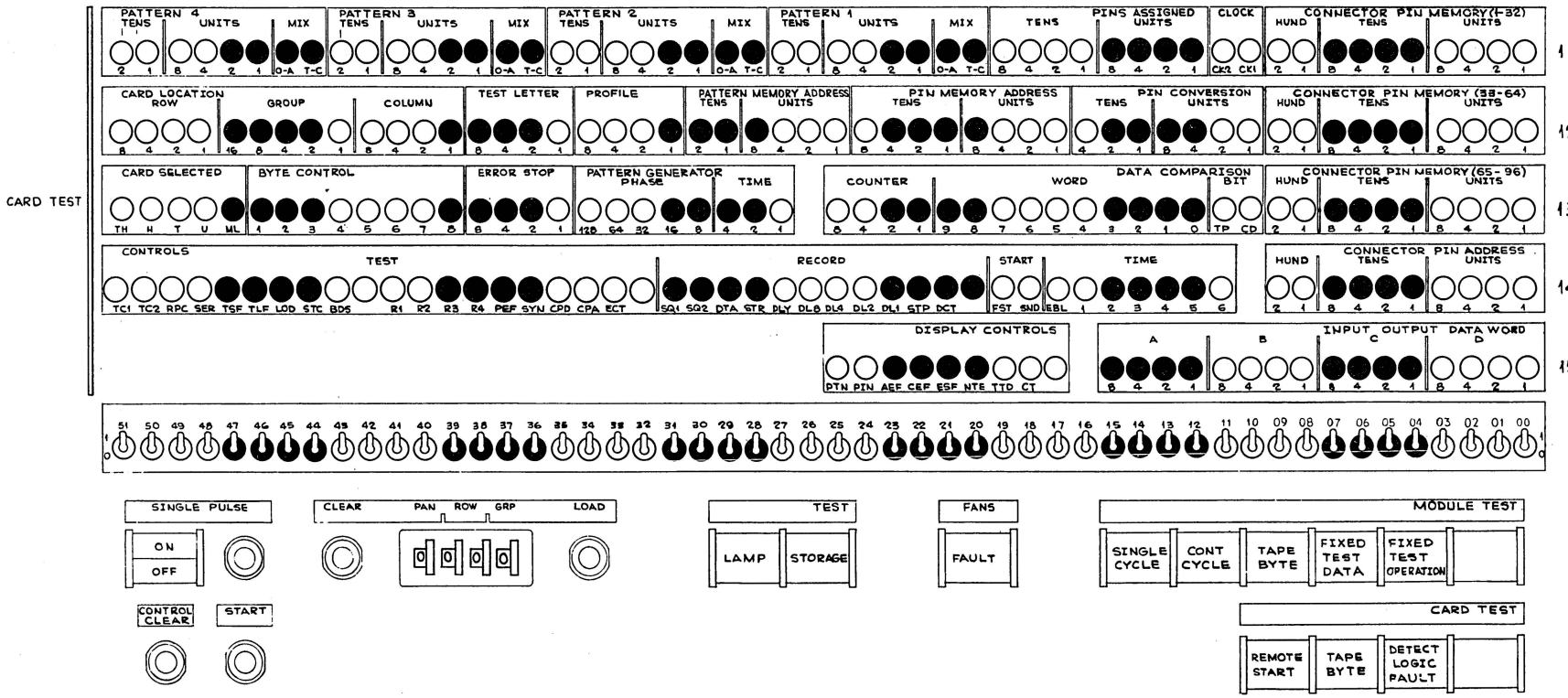


Figure VII-5-4. Maintenance Panel

CHAPTER VIII
FUNCTIONS OF THE MASTER CONTROL PROGRAM (MCP)

To make multiprogramming and multiprocessing a reality, a system must be capable of dynamically controlling its own resources and the scheduling of its jobs, and it must be capable of processing a number of jobs concurrently in less time than it takes to process the same jobs serially. The B 7700 system does these things by means of the master control program (MCP)--the software executive program that is the key to the effective, balanced use of the system. The B 7700 master control program is written in B 6700/B 7700 ESPOL, an extension of B 6700/B 7700 ALGOL.

By integrating users' object programs with the software-compatible B 7700 hardware system and with high-speed disk, the master control program optimizes the productivity of the B 7700 system. The master control program is, therefore, an essential part of the processing environment of the B 7700 system.

The integrative action of the master control program is achieved in the following three ways.

a. By its capability of coordinating the execution of many programs, or jobs, in the processor or processors.

b. By its capability of controlling both input and output so as to make optimal use of the relatively slow peripheral devices.

c. By its capability of taking executive action to meet virtually all processing conditions and to minimize the adverse effects of system degradation.

Thus, the overall rate and efficiency at which jobs can be processed under control of the master control program is increased, again, in three ways.

a. By increasing the speed of execution of individual users' programs. This increase in speed can be achieved by the use of a combination of several facilities, as follows:

   1. Parallel processing, or multiprocessing, with the introduction of more than one central processor module.

   2. Multiprogramming--the running of several jobs concurrently. The master control program maintains a list (ordered by priority) of jobs ready to run. When a running job must, for example, wait for an input or output operation to be completed, the master control program will start up the next job in the ready queue and restart the original job when the I/O operation has been completed and no jobs of higher priority are in the ready queue.

   3. Reentrant code--the means by which a single copy of a routine in main memory can be shared by several jobs.

4. Tasking--the processing in a coordinated manner of whole families of tasks.

b. By increasing the speed of data handling. For this purpose, two facilities are provided in the utility section of the master control program.

   1. Loadcontrol. This enables card input to be transferred to disk or tape. The card image files so formed are assigned to different pseudo card readers which are then treated by the master control program as if they were real physical card readers.

   2. Printer and punch backup. This enables output to be placed on tape or disk and then printed or punched out at a later, more convenient time.

c. By increasing the ease of operating the machine. Simple English-like operator attention and error messages, automatic assignment of labeled files to jobs without operator intervention, a simplified control card language, and other features help increase throughput on the B 7700 system.

Except in two areas--in the interface between the master control program and unique B 7700 hardware and in the area of failsoft--the B 7700 master control program is identical with the B 6700 master control program that has been operating successfully since 1969. A new approach to the software control of a data processing system is the B 7700 multilevel master control program, which is expected to provide users with many advantages not offered by the more traditional single-level master control program.

The multilevel master control program consists of a kernel, which has overall control of the B 7700 system and which is the sole interface between system software and system hardware, and one or more control programs, which run under control of the kernel and to which the kernel delegates many tasks of program supervision, system supervision, and input/output control.

There are two main reasons for adopting a multilevel approach to the software control of a data processing system. First, it is possible under control of the kernel to execute concurrently several control programs, each tailored to support a particular type of application, or job, be it batch work, testing of hardware modules, or time sharing. Each control program makes use of the strategies for resource allocation and scheduling most appropriate to a special kind of job and need not include irrelevant strategies. Thus, several control programs under the control of the kernel may share a hardware system, and each job running under control of a control program will benefit from the specialized facilities of the control program that controls it. Moreover, this arrangement permits the isolation of a user's production environment from, for example, an environment in which faulty hardware is being tested or an environment in which experimental system software is being debugged.

Second, by making the operating system more modular, it becomes more

understandable and more manageable, and thus, easier to write, maintain, and to extend. In fact, a user may write his own special control programs and still retain the use of the basic functions provided by the kernel and the standard control programs provided by Burroughs.

Although the general concepts presented in the following functional description of the B 7700 master control program apply as well to the multilevel version as to the single-level version, the details of implementation relate to the single-level master control program only.

SYSTEM STARTUP

In order to place the MCP in control of the system, the MCP code file must be loaded onto disk, starting at disk address 0 of the load disk unit. In addition, the MCP information table and the disk directory must be present on disk. When these initial conditions have been satisfied, the Halt-Load operation is used to read the first 8192 words of the MCP code file into core memory, and the system begins to execute the MCP.

The functions of loading the MCP code file to disk from magnetic tape and of creating or revising the MCP information table and the disk directory are accomplished by the System Loader program. This program is in the form of a card deck containing the machine code instructions, followed by data cards that specify parameters for the initialization. Items that may be specified include the types and number of peripherals available and their configuration in the I/O subsystem, the size of disk areas to be used for the disk directory and for overlay, the disk units to be used for backup or reconstruction, the tables to be displayed on particular supervisory consoles, the tape from which the MCP is to be loaded, and various run-time system options.

HARDWARE INTERRUPTS

The B 7700 processor hardware interrupt system is the primary interface between the MCP and the hardware. Hardware interrupts are generated automatically and under certain conditions by the B 7700 system and are handled by the MCP interrupt procedure. An interrupt is a means of diverting a processor from the job which it is doing if certain predetermined conditions occur. When a hardware interrupt has been processed by the MCP, the MCP will (if conditions then permit) reactivate the interrupted process.

When a processor is executing the interrupt handling procedure of the MCP, it is in control state, one of the two operating states of a processor. A processor can operate in either of two states: control state, used in executing the MCP, or normal state, used in executing user programs and certain MCP functions. In a multiprocessor system each processor handles its own interrupts; that is, all processors may be in control state at the same time.

Entry into control state occurs when the processor is started and as a result of certain interrupt conditions. In control state the processor can execute privileged instructions not available in normal state, and various classes of interrupts can be inhibited or allowed programmatically. Exit from control state into normal state occurs whenever

the MCP initiates a normal state program or exits back to a normal state program following an interrupt. In the latter case, user program return may not be to the program in process when the interrupt occurred.

Normal state excludes use of privileged instructions required by the MCP, permits hardware detection of invalid operators, and enforces memory protect and security facilities. Exit from normal state occurs as a result of an interrupt condition or by a call to a control state program, for example, to execute I/O. Many MCP functions can be run in normal state. Interrupts to a normal state MCP function can be enabled.

Hardware interrupts may be classified as internal and external interrupts. For internal (syllable dependent and syllable independent) interrupts, each processor in a B 7700 system is provided with a private, internal interrupt network. Internal interrupts associated with a processor are fed directly into this network and are stacked local to the processor. External interrupts, on the other hand, may be serviced by any processor in a system.

SYLLABLE DEPENDENT interrupts are detected by the processor operator logic. These include arithmetic error, presence bit, memory protect, and invalid operand interrupts. Except for arithmetic error interrupts, for which programmatic control may be supplied, and presence bit interrupts, interrupts of this group generally result in program termination.

SYLLABLE INDEPENDENT (alarm) interrupt conditions are not normally anticipated by the processor operator logic. They serve to inform the processor of some detrimental change in environment and can result from hardware failure as well as programming errors. These interrupts include those for a faulty read from memory, an invalid address, and an invalid program instruction word; all result in termination of the process involved.

EXTERNAL interrupt conditions are similar to the alarm interrupts, in that they are not anticipated by the operator logic. However, they do not normally require immediate action and do not necessarily result in termination of the program. These include interchannel and interval timer interrupts.

When a hardware interrupt condition occurs, the interrupted processor enters the control state, marks the stack, and inserts three words in the top of the stack. The first entry is an indirect reference word which points to a location that contains a PCW which points to the MCP hardware interrupt procedure. The first entry is followed by two interrupt parameters, P1 and P2, which contain information indicating the nature of the interrupt condition. When the processor enters the MCP hardware interrupt procedure, it remains in control state in order to disable external interrupts. The processor execution state (control or normal) is determined by the control bit of the PCW. When the control bit is on the processor will execute a procedure in control state. Otherwise, it will execute in normal state.

Upon entry to the hardware interrupt procedure the parameter P1 is analyzed to determine the type of interrupt which occurred. For some interrupts, such as presence bit interrupts, P2 contains additional information to be used by the interrupt procedure. Then the appropriate action is initiated.

After the interrupt procedure has been entered, the program base register is pointing at the interrupt procedure, the program index register and the program syllable register are pointing at the interrupt procedure entry point, and the return control word for the interrupt procedure's exit is pointing back to the object program's code.

STORAGE CONTROL

The MCP maintains records of storage availability through the use of memory links which are assigned within the areas they describe. Each type of memory link is linked to form a list which contains sufficient information for a single hardware operator to find the next memory link and all succeeding memory links. Memory areas are classified as in-use or available according to their current state.

Specifically, in-use memory links contain the stack number of the requesting process, the length of the in-use area, an availability bit set in the off position, a code indicating the usage of the area, links to the last previously allocated and next in-use areas, and so on. Available memory links contain the length of the area, an availability bit set in the on position, links to the next and last available areas, and so forth.

The MCP performs dynamic storage allocation by use of the environment control routine for all system storage media: main memory, magnetic disk, and system library magnetic tape. As a result of considering the different system storage media as a hierarchy of memory, the MCP controls allocation and deallocation of all system memory, regardless of the type.

Memory protection is provided for by a combination of hardware and software devices. One of the hardware features is automatic detection of an attempt by a program to index beyond its designated data area. Another is the use of one of the control bits in each word as a memory protect bit to prevent user programs from writing into words of memory which have the protect bit set. (The protect bit is set by the software.) Any attempt to perform such a write operation is inhibited, and an interrupt is generated, which results in termination of the program. Thus a user program cannot change program segments, data descriptors, or any program words or MCP tables during execution.

CONTROL OF JOBS

The MCP maintains control of jobs by the use of stacks, descriptors, and tables of system and process status.

One stack is associated with each job in the system. The stack, a contiguous area of memory, is assigned to a job to provide storage for basic program and data references. It also provides for temporary storage of data and job history. (Refer to chapter II for the details of the implementation of the stack in the B 7700.) When a job is activated on a processor, two high-

speed top-of-stack processor locations are linked to the job's stack memory area. This linkage is established by the stack-pointer register (S register), which contains the address of the last word placed in the stack. In addition, the 32-word stack buffer, an area of processor local IC memory, is made available to contain the top portion of the active stack, in order to provide quick access for stack manipulation by the processor.

Data are brought into and out of the stack through the top-of-stack locations according to the last-in, first-out principle. Total capacity of the top-of-stack locations is two operands. Loading a third operand into the top-of-stack locations causes the first operand to be pushed from the top-of-stack registers into the stack buffer. The stack-pointer register (S) is incremented by one as each word is placed into the stack or stack buffer and is decremented by one as each word is withdrawn and placed in the top-of-stack registers. As a result, the S register continually points to the last word placed into the job's stack.

A job's stack is bound, for memory protection, by two registers, the base-of-stack register (BOSR) and the limit-of-stack register (LOSR). The contents of BOSR define the base of the stack, and the LOSR defines the upper limit of the stack. The job is interrupted if the S register is set to the value contained in either LOSR or BOSR.

Descriptors are words used to locate data and program areas in memory and to describe these areas for control purposes. Descriptors are the only words containing absolute addresses which can be used by a user's program; however, the user's program cannot alter them. Descriptors are divided into three categories: data, string, and segment.

DATA descriptors are used for referring to data areas, including input/output buffer areas. The data descriptor defines an area of memory starting at the base address contained in the descriptor. The size of the memory area in number of words is contained in the length field of the descriptor. Data descriptors may directly reference any memory word address.

STRING descriptors refer to data areas organized as 4-, 6-, or 8-bit characters. The descriptor defines an area of memory starting at the base address contained in the descriptor. The size of the memory area is defined by the length field.

SEGMENT descriptors are used to locate program segments. These descriptors contain either the main memory or disk file address of a particular segment. All programs are entered and exited through the segment descriptors common in the segment dictionary stack; all references to those descriptors are relative. Entrance to or removal of any given program segment from memory is achieved by changing the presence bit in that segment descriptor. No stack search of any kind is required.

The MCP also maintains tables that summarize system and process status. The mix table contains the priority, status (scheduled, active, or suspended), and mix index of each job that has been entered in the system. The peripheral unit table has an entry for each peripheral unit in the

system. Each entry contains the status of the corresponding unit and the file associated with that unit.

Scheduling and Initiation of Jobs

The sequence of jobs to be run and the optimal program mix considering the priority ratings and system requirements of each object program and considering the present system configuration are determined by the scheduling routine of the MCP. The MCP incorporates a dynamic scheduling algorithm, that is, one which reschedules the job sequence whenever a higher priority job is introduced into the system. Job priority may be programmer-defined by use of the PRIORITY statement. If no priority is specified by the programmer, a default value of one-half the maximum allowable priority is assigned by the MCP.

The calculation of the priorities is performed in a well-isolated section of the MCP. Thus, the user may easily tailor the Burroughs-supplied priority algorithms to his specific requirements.

As each job is read from the system input unit (card reader or pseudo card reader, i.e., magnetic tape or disk), the control card interpreting procedure, CONTROLCARD, makes an entry into the sheet queue to schedule each batch-mode process. The sheet queue is a linked list of processes which await execution. Each entry in the sheet queue is a partially built process stack. The information contained in this stack includes the estimated amount of main memory required by the process, priority, time of entry into the schedule, size and location of code segments, working storage stack size, and size and location of the process stack information. After CONTROLCARD completes its tasks and if sufficient system resources are free, the entry is moved from the sheet queue to a queue called the ready queue.

When sufficient system resources exist to allow another job into the mix, called RUN is started. RUN makes the segment dictionary for the job present in main memory and transfers control to the job.

Real-time and time-sharing applications entering the system by way of the data communication facilities merely become additions to the multiprogramming mix.

Execution of Jobs

As soon as control is first transferred to a new job, an interrupt may occur because the outer block code segment is generally not present in main memory. This interrupt is handled by the PRESENCEBIT procedure of the MCP. PRESENCEBIT is entered and the following actions occur in order to bring the segment into memory: (1) PRESENCEBIT calls GETSPACE to allocate an area in main memory for the code segment; (2) after an area is allocated, PRESENCEBIT calls DISKIO, the disk input/output procedure, and waits for notification that the segment has been read in; and (3) DISKIO links the request into the I/O queue. Upon completion of the disk I/O, PRESENCEBIT is notified that the segment is now available. PRESENCEBIT marks the segment descriptor present and exits back to the job at the point of interruption, and the job continues to run.

A program residing in memory occupies separately allocated areas; that is, each part of the program may reside anywhere in memory. The actual address is determined by the MCP. Also, the various parts are not necessarily assigned to contiguous memory areas. Registers within the processor and descriptors in the stack indicate the bases of the various areas during the execution of a program.

The separately allocated areas of a program are: (1) the program segments--sequences of instructions performed by the processor in executing the program; (2) the segment dictionary, a table containing one word for each program segment; this word tells whether the program segment is in main memory or on the disk, and gives its corresponding main memory or disk address; (3) the stack, which contains all the variables associated with the program, including control words that indicate the dynamic status of the job as it is being executed; (4) data areas used by the program, which are referenced by data descriptors or string descriptors in the program's stack; and (5) the MCP stacks and segment dictionary, which contain variables pertinent to the MCP and the MCP segment dictionary entries.

As a job runs, additional segments of program code and data will be needed. The job stack contains the storage locations for simple variables and array data descriptors, but program code segments and array rows are assigned their own areas of memory. This assignment of separate memory areas for code segments and array rows allows segments and data to be absent from main memory until they are actually needed. Thus, in the B 7700 system a reference to data or code through a data descriptor or a segment descriptor causes the processor to check the presence bit in the descriptor.

If the presence bit is off, an interrupt occurs which transfers control to PRESENCEBIT. The nonpresent descriptor is passed as a parameter. PRESENCEBIT reads the address field of the descriptor and calls the GETSPACE procedure to allocate an area in main memory for the code segment. Parameters are supplied to GETSPACE so that an adequate-sized contiguous area of memory may be reserved for a particular stack. After GETSPACE satisfies the request for core space, it returns the memory address of the area it has allocated, and PRESENCEBIT causes the information to be read from disk into memory. When the disk read is finished, PRESENCEBIT stores the memory address of the information into the address field of the descriptor, turns the presence bit on, and updates the descriptor in the process stack. PRESENCEBIT then returns control to the interrupted process, and the information is accessed again by the process. Now the information is present in memory; the information is obtained and the process execution continues in the normal manner.

The storage required for the referenced data or code may be allocated at the front or rear of an adequate-sized area and marked as overlayable or nonoverlayable. When an in-use area is allocated, it is linked to the previously allocated in-use area by the left-off link and pointer fields in the memory links. These fields constitute the left-off list. A reference word pointing to the oldest entry in the left-off list

allows the chronological history of in-use memory areas to be determined.

When there is insufficient available memory to satisfy a particular request, the overlay mechanism is invoked. The left-off list is searched, starting at the overlayable area that has been allocated for the longest period of time. If this area, combined with any adjacent available area, is adequate to satisfy the request, it is overlaid. Otherwise, allocated areas with lower starting addresses are considered.

If the request is satisfied and the area found is larger than the required size, the unused portion is made available by linking it to the available list. If the request is not satisfied, the next oldest overlayable area is obtained and the left-off list is searched as described above. This process is repeated until the left-off list has been exhausted. If the request cannot be satisfied, a no memory condition exists.

Software Interrupts and Events

Software interrupts are programmatically defined for use by the MCP and object program processes. Software interrupts allow processes to communicate with each other and with the MCP.

Software interrupts allow a process to stop running (thereby releasing the processor) until a specified event occurs, or continue running and be interrupted if the event does occur. A software interrupt occurs when a process is interrupted by the direct action of some other process.

A process can be interrupted if it has an interrupt declaration (statement) within its scope.

A process may invoke the occurrence of an event by means of the CAUSE statement. The MCP scans the event interrupt queue to determine if the interrupt has been enabled. If the interrupt is not enabled and the event is caused, no action is taken by the MCP on that process, and it looks at the next process stack in the queue.

If interrupts are enabled in the next stack, the MCP makes an entry in the software interrupt queue. This queue is ordered by stack number. If the stack is active, that is, if another processor is working in the stack, the MCP will interrupt that processor with an interchannel interrupt. Next, the MCP forces a transfer of control to the statement related to the interrupt declaration. Upon completion of this statement, the process will return to its previous point of control unless a transfer of control is specified in the interrupt statement. In this case the process will not return the point of control before the interrupt but will transfer control as specified in the interrupt statement.

As the MCP scans the event interrupt queue finding enabled interrupts in inactive stacks, it makes an entry in the software interrupt queue, doing nothing with that stack until it becomes active. Immediately after making that stack active, the MCP checks the software interrupt queue to see if there is an interrupt pointing to that stack. If an interrupt is found, the MCP forces a transfer of control to the statement referred to by the interrupt declar-

ation. Upon completion of the statement, control is transferred as described above.

Termination of Jobs

When the execution of a job is terminated, the following actions occur: (1) any outstanding I/O requests are completed, if possible, and any open files are closed, the units released, and the buffer areas are returned to the available memory table; (2) all overlayable disk areas allocated to the job are returned to the available disk table; (3) all job object code and data array areas of main memory are returned to the available memory table; (4) an end-of-job entry is made in the system log for the job; and (5) the job's stack is linked into the terminate queue.

INPUT/OUTPUT CONTROL

All input/output operations on the B 7700 system are performed by the MCP. The MCP automatically assigns peripheral units to symbolic files whenever possible in order to minimize the amount of operator attention needed by each job. When an input file is requested by a job, the MCP searches its tables for the appropriate peripheral unit which contains the file requested. If the file name specified by the job is found on a particular unit, that unit is marked in use and assigned to the job. Output files requested by a job are automatically assigned by the MCP if a suitable unit exists for the file. In the case of disk files, a disk file directory entry is made and the needed disk space is allocated for the file.

File Handling

In order for the MCP to associate peripheral units with symbolic files, the compilers that run on the B 7700 system must furnish the following information about files to the MCP: the symbolic file name, the actual file name (file title), the peripheral type (disk, magnetic tape, card, paper tape, etc.), the access type (serial or random), the file mode (alpha, binary, etc.), the buffer size, the number of buffers, and the logical record size. The actual file name is the file title which is associated with the unit that contains the file or the title in the disk file header. The actual file name will be identical with the symbolic file name unless otherwise specified by label equation control statements.

In order to allow dynamic specification of actual file names for a file, three tables are necessary: a process parameter block, a label equation block, and a file information block. The process parameter block is created by CONTROLCARD for all files in a job. It contains the symbolic file name and any compilations or execution time label equation information specified for this process. The label equation block and the file information block are created by the compiler and maintained by I/O functions for each file in a process. The label equation block contains the current label equation and other file attribute information for a particular file, including any programmatic specification of file attributes. The file information block contains frequently used information concerning the file, such as the type of access required, type of unit assigned, physical unit being used,

and attributes which depend upon the type of unit assigned. Incorporation of the file attributes in the file information block and label equation block allows modification of file specifications such as buffer size and blocking factors, at program execution time, without recompilation of the program.

Transfer of Data

Object program I/O operations on the B 7700 system involve the automatic transfer of logical records between a file and a job. A logical record consists of the information the job references with one Read or Write statement. The size of a logical record does not necessarily coincide with the size of the physical record or block accessed by the hardware I/O operations. When a physical record contains more than one logical record, the file is referred to as a blocked file.

When a file is accessed by a job, a physical record is written from or read to a memory area known as a buffer area for the file. If the file is blocked, the MCP maintains a record pointer into the buffer. This pointer is used by the process to access the current logical record. If the next record is not already present in a buffer, then the MCP automatically performs the required I/O operation.

Multiple buffers may be used to effectively increase throughput for jobs that require groups of physical records at one time. Since the MCP performs all object program I/O action, a job with multiple buffers allocated for a file allows the MCP to perform I/O operations independent of the status of the job. The determination of the number of buffers required for efficient execution of a job depends on the type of files being used, the particular hardware configuration being used, the processing characteristics of the job, the memory requirements of the job, and the mix of jobs which are typically multiprocessing. The MCP attempts to keep all input buffers full and all output buffers empty for each job, regardless of status, thereby minimizing the time that a process is suspended waiting for an I/O operation to be completed.

Data Communications

The MCP provides extensive data communication facilities, including time-sharing, remote computing, and remote inquiring. No terminal device interfaces directly with the central system. Instead, the necessary linkage is provided through a communications line, adapter and multiplexing devices, and the data communications processor.

Those aspects of the data communications system that are oriented toward applications are handled by the message control system (MCS) program. These aspects include remote file maintenance and job control. In addition, the message control system coordinates interprogram communications and provides message-switching capabilities. A single remote station may communicate with other remote stations or more than one object job.

The MCS may (1) accept input from a variable number of remote stations through a program communication file in core; (2) react to the activation and deactivation of stations (for example, it may allow a dial-line, ring indicator to be answered

and send the first message)); (3) perform command and edit functions as required by the input data stream; (4) perform command functions upon occurrence of exception conditions, including controlling subsequent I/O of other devices attached to the line; (5) initiate object jobs as independent processes and handle certain command requests from object programs such as file open attachment of files to given lines; and (6) maintain file security restrictions and check remote user security.

COMMUNICATION BETWEEN USER AND MCP

Communication between the user of the B 7700 system and the MCP is accomplished with a combination of display units, control units (display units with associated keyboards), control cards, and a comprehensive system log.

The status of the system and of the jobs in progress is presented on the display units. Specific questions requiring short answers may be entered by use of the keyboard. These questions and answers are displayed as they occur. Also, by entering the appropriate keyboard messages, various tables may be called for display. These tables include the job mix, peripheral unit, label, and disk directory tables.

The operator communicates directly with the MCP by the use of input and output messages entered and received at the control units. The input messages include any control statement allowed on a control card, messages to enter jobs into the mix and to eliminate jobs from the mix, and messages to reactivate jobs that have been suspended. Output messages pertain to various functional areas of the MCP, to users' programs, and to system hardware modules.

A user submits a job to the system as a set of control cards and a source language deck. Alternatively, he may submit only a set of control cards or enter control statements at the input keyboard if he has previously stored on disk the programs that he wishes to run and has entered their names in the disk directory following an error-free compilation.

For a job requiring compilation, the first control card must be a compile statement, which specifies the compiler to be used and the type of compilation to be made. There are three forms: compile and execute, compile for the library, and compile for syntax check. The other types of control cards may be used for all jobs whether they do or do not require compilation. These include an execute statement, process time statement, priority statement, core requirement statement, I/O time statement, and I/O unit statements which associate file labels with particular I/O units.

The MCP maintains on disk a system log, which is a record of all activities on the system. Besides system error and maintenance statistics, the log makes available to the user such data as the processing time for each job, the time at which each job was started, its elapsed running time, and its actual processor time.

APPENDIX A
ORDER OF MAGNITUDE CHART

REGISTER BIT SET	DECIMAL	DECIMAL RECIPROCAL	HEX.	OCTAL	BINARY
0	1	1.0	16^0	8^0	2^0
1	2	0.5			
2	4	0.25			
3	8	0.125		8^1	2^3
4	16	0.0625	16^1		
5	32	0.03125			
6	64	0.015625		8^2	2^6
7	128	0.0078125			
8	256	0.00390625	16^2		
9	512	0.001953125		8^3	2^9
10	1024	0.0009765625			
11	2048	0.00048828125			
12	4096	0.000244140625	16^3	8^4	2^{12}
13	8192	0.0001220703125			
14	16384	0.00006103515625			
15	32768	0.000030517578125		8^5	2^{15}
16	65536	0.0000152587890625	16^4		
17	131072	0.00000762939453125			
18	262144	0.00000381469726562 5		8^6	2^{18}
19	524288	0.0000019073486328125			
20	1048576	0.0000009536743164062 5	16^5		
21	2097152	0.0000004768371582031 25		8^7	2^{21}
22	4194304	0.0000002384185791015625			
23	8388608	0.0000001192092895507812 5			
24	16777216	0.0000000596046447753906 25	16^6	8^8	2^{24}
25	33554432	0.0000000298023223876953125			
26	67108864	0.0000000149011611938476562 5			
27	134217728	0.0000000074505805969238281 25		8^9	2^{27}
28	268435456	0.0000000037252902984619140625	16^7		
29	536870912	0.0000000018626451492309570312 5			
30	1073741824	0.0000000009313225746154785156 25		8^{10}	2^{30}
31	2147483648	0.0000000004656612873077392578125			
32	4294967296	0.0000000002328306436538696289062 5	16^8		
33	8589934592	0.0000000001164153218269348144531 25		8^{11}	2^{33}
34	17179869184	0.0000000000582076609134674072265625			
35	34359738368	0.0000000000291038304567337036132812 5			
36	68719476736	0.0000000000145519152283668518066406 25	16^9	8^{12}	2^{36}
37	137438953472	0.0000000000072759576141834259033203125			
38	274877906944	0.0000000000036379788070917129516601562 5			
*	549755813887			8^{13}	2^{39}
39	549755813888	0.0000000000018189894035458564758300781 25			

* FIRST 39 BITS SET. (MAXIMUM INTEGER VALUE ALLOWED).

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APPENDIX B
HEXADECIMAL ADDITION TABLE

Hexadecimal Addition Table

+	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10
2	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11
3	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12
4	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13
5	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14
6	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15
7	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16
8	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17
9	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18
A	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19
B	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A
C	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

APPENDIX C
HEXADECIMAL TO DECIMAL CONVERSION TABLES

Table A and table B provide for direct conversion from hexadecimal to decimal numbers in the range of:

Hexadecimal

00000 to FFFFF

or

Decimal

0 to 1048575

Table A provides the decimal value of the first 2 digits of a 5-digit hexadecimal number (nn---), and the table B provides the decimal value of the last 3 digits of a 5-digit hexadecimal number (--NNN).

Hexadecimal-Decimal Conversion Table A

x	0x	1x	2x	3x	4x	5x
0	0	65536	131072	196608	262144	327680
1	4096	69632	135168	200704	266240	331776
2	8192	73728	139264	204800	270336	335872
3	12288	77824	143360	208896	274432	339968
4	16384	81920	147456	212992	278528	344064
5	20480	86016	151552	217088	282624	348160
6	24576	90112	155648	221184	286720	352256
7	28672	94208	159744	225280	290816	356352
8	32768	98304	163840	229376	294912	360448
9	36864	102400	167936	233472	299008	364544
A	40960	106496	172032	237568	303104	368640
B	45056	110592	176128	241664	307200	372736
C	49152	114688	180224	245760	311296	376832
D	53248	118784	184320	249856	315392	380928
E	57344	122880	188416	253952	319488	385024
F	61440	126976	192512	258048	323584	389120

x	6x	7x	8x	9x	Ax	Bx
0	393216	458752	524288	589824	655360	720896
1	397312	462848	528384	593920	659456	724992
2	401408	466944	532480	598016	663552	729088
3	405504	471040	536576	602112	667648	733184
4	409600	475136	540672	606208	671744	737280
5	413696	479232	544768	610304	675840	741376
6	417792	483328	548864	614400	679936	745472
7	421888	487424	552960	618496	684032	749568
8	425984	491520	557056	622592	688128	753664
9	430080	495616	561152	626688	692224	757760
A	434176	499712	565248	630784	696320	761856
B	438272	503808	569344	634880	700416	765952
C	442368	507904	573440	638976	704512	770048
D	446464	512000	577536	643072	708608	774144
E	450560	516096	581632	647168	712704	778240
F	454656	520192	585728	651264	716800	782336

x	Cx	Dx	Ex	Fx
0	786432	851968	917504	983040
1	790528	856064	921600	987136
2	794624	860160	925696	991232
3	798720	864256	929792	995328
4	802816	868352	933888	999424
5	806912	872448	937984	1003520
6	811008	876544	942080	1007616
7	815104	880640	946176	1011712
8	819200	884736	950272	1015808
9	823296	888832	954368	1019904
A	827392	892928	958464	1024000
B	831488	897024	962560	1028096
C	835584	901120	966656	1032192
D	839680	905216	970752	1036288
E	843776	909312	974848	1040384
F	847872	913408	978944	1044480

HEXADECIMAL-DECIMAL CONVERSION TABLE B

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
010	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
020	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
030	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
040	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
050	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
060	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
070	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
080	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
090	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
0A0	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
0B0	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
0C0	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
0D0	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
0E0	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
0F0	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
100	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
110	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
120	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
130	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
140	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
150	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
160	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
170	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383

HEXADECIMAL-DECIMAL CONVERSION TABLE B (Cont)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
180	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
190	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
1A0	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
1B0	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
1C0	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
1D0	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
1E0	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
1F0	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
200	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
210	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
220	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
230	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
240	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
250	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
260	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
270	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
280	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
290	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
2A0	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687
2B0	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
2C0	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
2D0	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
2E0	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
2F0	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
300	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
310	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
320	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
330	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
340	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
350	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
360	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
370	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
380	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
390	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
3A0	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943
3B0	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
3C0	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
3D0	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
3E0	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007
3F0	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
400	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
410	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
420	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
430	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
440	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
450	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
460	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
470	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
480	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
490	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A0	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B0	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C0	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D0	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E0	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F0	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
500	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
510	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
520	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
530	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
540	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
550	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
560	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
570	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
580	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
590	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A0	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B0	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C0	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D0	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E0	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F0	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
600	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
610	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
620	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
630	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
640	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
650	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
660	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
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7A0	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B0	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D0	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F0	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047
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AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
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C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
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CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
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D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
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FE0	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF0	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

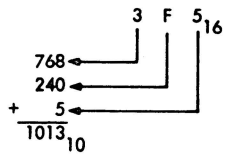
APPENDIX D
DECIMAL-HEXADECIMAL CONVERSION TABLE

Decimal-Hexadecimal Conversion Table

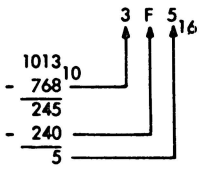
(DECIMAL = H x 16^{I})

H ↓ I → 6	5	4	3	2	1	0
1	16777216	1048576	65536	4096	256	16	1
2	33554432	2097152	131072	8192	512	32	2
3	50331648	3145728	196608	12288	768	48	3
4	67108864	4194304	262144	16384	1024	64	4
5	83886080	5242880	327680	20480	1280	80	5
6	100663296	6291456	393216	24576	1536	96	6
7	117440512	7340032	458752	28672	1792	112	7
8	134217728	8388608	524288	32768	2048	128	8
9	150994944	9437184	589824	36864	2304	144	9
A	167772160	10485760	655360	40960	2560	160	10
B	184549376	11534336	720896	45056	2816	176	11
C	201326592	12582912	786432	49152	3072	192	12
D	218103808	13631488	851968	53248	3328	208	13
E	234881024	14680064	917504	57344	3584	224	14
F	251658240	15728640	983040	61440	3840	240	15

HEXADECIMAL TO DECIMAL



DECIMAL TO HEXADECIMAL



Hexadecimal to Decimal. Find the decimal value for each hexadecimal digit according to its position. Add these to obtain the decimal equivalent.

Decimal to Hexadecimal. Find the next lower decimal number and its Hexadecimal equivalent. Subtract and use difference to find the next decimal value and hexadecimal equivalent until the complete number is developed.

APPENDIX E
COLLATING INFORMATION

All characters are collated according to their internal binary value. Because the B 7700 has the capability of representing characters internally in BCL, EBCDIC, or USASCII, and because characters are collated according to their internal representation (not necessarily the same as their external mode) a variety of collating sequences is possible. The following table may be used to determine the applicable collating sequence.

Input Mode	Output Mode	Internal Mode	Collating Sequence
BCL	BCL	BCL	BCL (BCL internal)
BCL	EBCDIC	EBCDIC	BCL Translated to EBCDIC
BCL	BCL	EBCDIC	BCL Translated to EBCDIC
EBCDIC	EBCDIC	EBCDIC	EBCDIC
EBCDIC	BCL	EBCDIC	BCL Translated to EBCDIC
EBCDIC	USASCII	EBCDIC	USASCII Translated to EBCDIC
USASCII	USASCII	USASCII	USASCII
USASCII	EBCDIC	EBCDIC	USASCII Translated to EBCDIC
USASCII	BCL	USASCII	BCL Translated to USASCII
USASCII	EBCDIC	USASCII	USASCII Translated to EBCDIC

CHARACTER REPRESENTATION

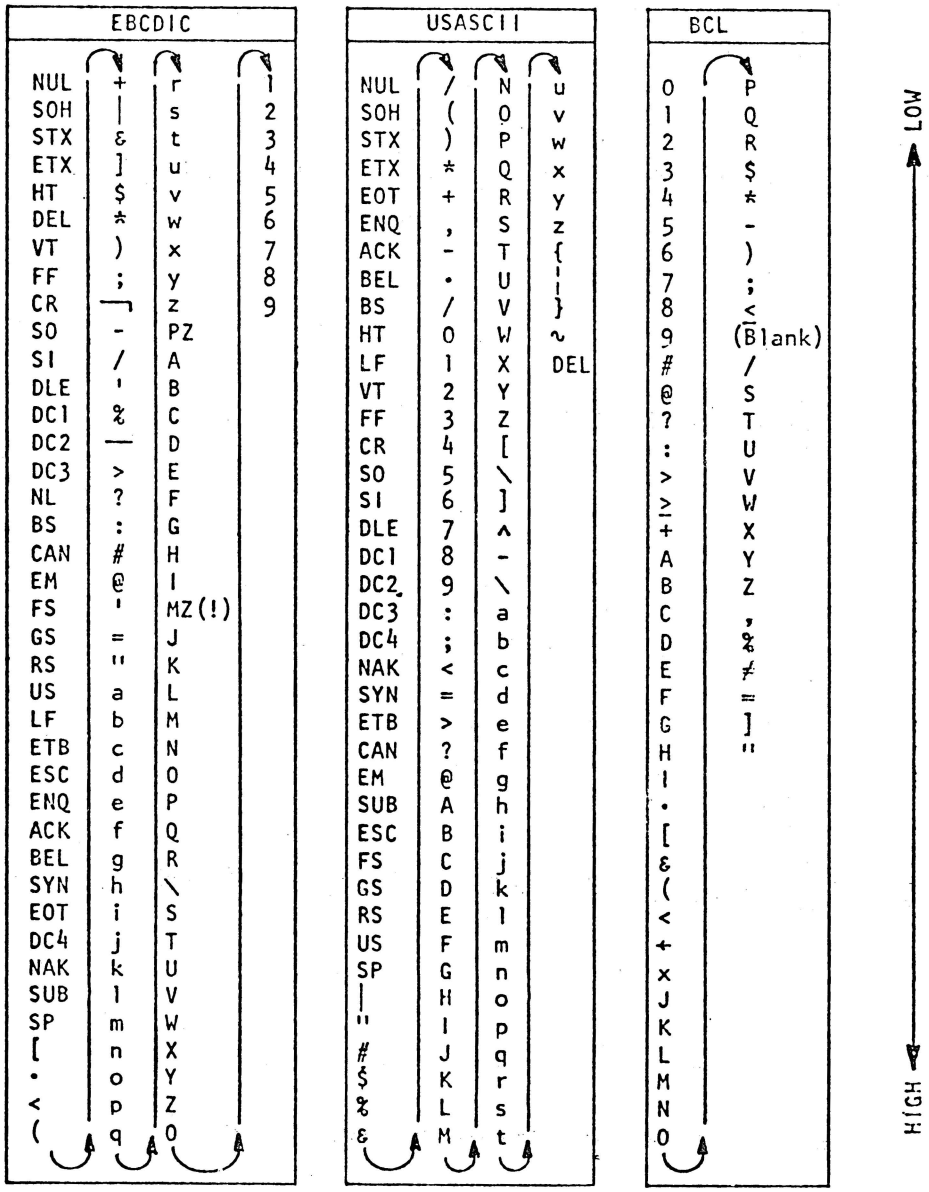
The BCL, EBCDIC, and USASCII graphics are the same except as follows:

BCL	EBCDIC	USASCII
≥	' (single quote)	'
x (multiply)	! or | or MZ	}
≤	¬ (not)	^
≠	_ (underscore)	
←	| (or)	!
↑	PZ (+)	{
↓	<	
<	>	
>	+	
	-	

A BCL plus sign is never translated to an EBCDIC PZ (plus zero) sign, although the EBCDIC PZ is translated to a BCL plus sign.

EBCDIC 1110 0000 is translated to BCL 00 0000 with an additional flag bit on the next to most significant bit line (7th bit). As the print drums have 64 graphics and space this signal can be used to print the 64th graphic. The 64th graphic is a "CR" for BCL drums and a "¢" for EBCDIC drums.

COLLATING SEQUENCES



EBCDIC COLLATING SEQUENCE

EBCDIC Character	Hex. Code	Internal Code	Card Code Zone Number
NUL	00	0000 0000	12-0-9- 8-1
SOH	01	0000 0001	12-9- 1
STX	02	0000 0010	12-9- 2
ETX	03	0000 0011	12-9- 3
HT	05	0000 0101	12-9- 5
DEL	07	0000 0111	12-9- 7
VT	0B	0000 1011	12-9- 8-3
FF	0C	0000 1100	12-9- 8-4
CR	0D	0000 1101	12-9- 8-5
SO	0E	0000 1110	12-9- 8-6
SI	0F	0000 1111	12-9- 8-7
DLE	10	0001 0000	12-11-9- 8-1
DC1	11	0001 0001	11-9- 1
DC2	12	0001 0010	11-9- 2
DC3	13	0001 0011	11-9- 3
NL	15	0001 0101	11-9 5
BS	16	0001 0110	11-9- 6
CAN	18	0001 1000	11-9- 8
EM	19	0001 1001	11-9- 8-1
FS	1C	0001 1100	11-9- 8-4
GS	1D	0001 1101	11-9- 8-5
RS	1E	0001 1110	11-9- 8-6
US	1F	0001 1111	11-9- 8-7
LF	25	0010 0101	0-9- 5
ETB	26	0010 0110	0-9- 6
ESC	27	0010 0110	0-9- 7
ENQ	2D	0010 1101	0-9- 8-5
ACK	2E	0010 1110	0-9- 8-6
BEL	2F	0010 1111	0-9- 8-7
SYN	32	0011 0010	9- 2
EOT	37	0011 0111	9- 7
DC4	3C	0011 1100	9- 8-4
NAK	3D	0011 1101	9- 8-5
SUB	3F	0011 1111	9- 8-7
SP	40	0100 0000	(No Punches)
[	4A	0100 1010	12- 8-2
.	4B	0100 1011	12- 8-3
<	4C	0100 1100	12- 8-4
(	4D	0100 1101	12- 8-5
+	4E	0100 1110	12- 8-6
| (↵)	4F	0100 1111	12- 8-7

LOW ▲ ▼ HIGH

EBCDIC COLLATING SEQUENCE (Cont)

EBCDIC Character	Hex. Code	Internal Code	Card Code Zone	Number
&	50	0101 0000	12-	-
]	5A	0101 1010	11-	8-2
$	5B	0101 1011	11-	8-3
*	5C	0101 1100	11-	8-4
)	5D	0101 1101	11-	8-5
;	5E	0101 1110	11-	8-6
¬ (≤)	5F	0101 1111	11-	8-7
- (Dash)	60	0110 0000	11-	-
/	61	0110 0001	0-	1
, (Comma)	6B	0110 1011	0-	8-3
%	6C	0110 1100	0-	8-4
_ (≠)	6D	0110 1101	0-	8-5
>	6E	0110 1110	0-	8-6
?	6F	0110 1111	0-	8-7
:	7A	0111 1010	-	8-2
#	7B	0111 1011	-	8-3
@	7C	0111 1100	-	8-4
' (≥)	7D	0111 1101	-	8-5
=	7E	0111 1110	-	8-6
"	7F	0111 1111	-	8-7
a	81	1000 0001	12-0-	1
b	82	1000 0010	12-0-	2
c	83	1000 0011	12-0-	3
d	84	1000 0100	12-0-	4
e	85	1000 0101	12-0-	5
f	86	1000 0110	12-0-	6
g	87	1000 0111	12-0-	7
h	88	1000 1000	12-0-	8
i	89	1000 1001	12-0-	9
j	91	1001 0001	12-11-	1
k	92	1001 0010	12-11-	2
l	93	1001 0011	12-11-	3
m	94	1001 0100	12-11-	4
n	95	1001 0101	12-11-	5
o	96	1001 0110	12-11-	6
p	97	1001 0111	12-11-	7
q	98	1001 1000	12-11-	8
r	99	1001 1001	12-11-	9

LOW ↑ ↓ HIGH

EBCDIC COLLATING SEQUENCE (Cont)

EBCDIC Character	Hex. Code	Internal Code	Card Code Zone Number	
s	A2	1010 0010	11-0-	2
t	A3	1010 0011	11-0-	3
u	A4	1010 0100	11-0-	4
v	A5	1010 0101	11-0-	5
w	A6	1010 0110	11-0-	6
x	A7	1010 0111	11-0-	7
y	A8	1010 1000	11-0-	8
z	A9	1010 1001	11-0-	9
PZ (+)	C0	1100 0000	12-0	
A	C1	1100 0001	12-	1
B	C2	1100 0010	12-	2
C	C3	1100 0011	12-	3
D	C4	1100 0100	12-	4
E	C5	1100 0101	12-	5
F	C6	1100 0110	12-	6
G	C7	1100 0111	12-	7
H	C8	1100 1000	12-	8
I	C9	1100 1001	12-	9
MZ (!)	D0	1101 0000	11-	0
J	D1	1101 0001	11-	1
K	D2	1101 0010	11-	2
L	D3	1101 0011	11-	3
M	D4	1101 0100	11-	4
N	D5	1101 0101	11-	5
O	D6	1101 0110	11-	6
P	D7	1101 0111	11-	7
Q	D8	1101 1000	11-	8
R	D9	1101 1001	11-	9
\ (CR) (¢)	E0	1110 0000	0-	8-2
S	E2	1110 0010	0-	2
T	E3	1110 0011	0-	3
U	E4	1110 0100	0-	4
V	E5	1110 0101	0-	5
W	E6	1110 0110	0-	6
X	E7	1110 0111	0-	7
Y	E8	1110 1000	0-	8
Z	E9	1110 1001	0-	9

LOW ▲ ▼ HIGH

EBCDIC COLLATING SEQUENCE (Cont)

EBCDIC Character	Hex. Code	Internal Code	Card Code Zone	Number
0	F0	1111 0000	-	0
1	F1	1111 0001	-	1
2	F2	1111 0010	-	2
3	F3	1111 0011	-	3
4	F4	1111 0100	-	4
5	F5	1111 0101	-	5
6	F6	1111 0110	-	6
7	F7	1111 0111	-	7
8	F8	1111 1000	-	8
9	F9	1111 1001	-	9

LOW ▲ ▼ HIGH

BCL COLLATING SEQUENCE (BCL INTERNAL)

BCL Character	BCL Octal	BCL Hex	BCL Internal BA 8421	BCL External BA 8421	Card Code Zone	Number
0	00	00	00 0000	00 1010	-	0
1	01	01	00 0001	00 0001	-	1
2	02	02	00 0010	00 0010	-	2
3	03	03	00 0011	00 0011	-	3
4	04	04	00 0100	00 0100	-	4
5	05	05	00 0101	00 0101	-	5
6	06	06	00 0110	00 0110	-	6
7	07	07	00 0111	00 0111	-	7
8	10	08	00 1000	00 1000	-	8
9	11	09	00 1001	00 1001	-	9
#	12	0A	00 1010	00 1011	-	8-3
@	13	0B	00 1010	00 1100	-	8-4
?	14	0C	00 1100	00 0000	All other card codes	
:	15	0D	00 1101	00 1101	-	8-5
>	16	0E	00 1110	00 1110	-	8-6
≥	17	0F	00 1111	00 1111	-	8-7
+	20	10	01 0000	11 1010	12	0
A	21	11	01 0001	11 0001	12	1
B	22	12	01 0010	11 0010	12	2
C	23	13	01 0011	11 0011	12	3
D	24	14	01 0100	11 0100	12	4
E	25	15	01 0101	11 0101	12	5
F	26	16	01 0110	11 0110	12	6
G	27	17	01 0111	11 0111	12	7

LOW ▲ ▼ HIGH

BCL COLLATING SEQUENCE (BCL INTERNAL) (Cont)

BCL Character	BCL Octal	BCL Hex	BCL Internal BA 8421	BCL External BA 8421	Card Code Zone	Card Code Number
H	30	18	01 1000	11 1000	12	8
I	31	19	01 1001	11 1001	12	9
.	32	1A	01 1010	11 1011	12	8-3
[	33	1B	01 1011	11 1100	12	8-4
&	34	1C	01 1100	11 0000	12	-
(	35	1D	01 1101	11 1101	12	8-5
<	36	1E	01 1110	11 1110	12	8-6
←	37	1F	01 1111	11 1111	12	8-7
x(Mult.)	40	20	10 0000	10 1010	11	0
J	41	21	10 0001	10 0001	11	1
K	42	22	10 0010	10 0010	11	2
L	43	23	10 0011	10 0011	11	3
M	44	24	10 0100	10 0100	11	4
N	45	25	10 0101	10 0101	11	5
O	46	26	10 0110	10 0110	11	6
P	47	27	10 0111	10 0111	11	7
Q	50	28	10 1000	10 1000	11	8
R	51	29	10 1001	10 1001	11	9
$	52	2A	10 1010	10 1011	11	8-3
*	53	2B	10 1011	10 1100	11	8-4
-	54	2C	10 1100	10 0000	11	-
)	55	2D	10 1101	10 1101	11	8-5
;	56	2E	10 1110	10 1110	11	8-6
≤	57	2F	10 1111	10 1111	11	8-7
Blank	60	30	11 0000	01 0000	-	-
/	61	31	11 0001	01 0001	0	1
S	62	32	11 0010	01 0010	0	2
T	63	33	11 0011	01 0011	0	3
U	64	34	11 0100	01 0100	0	4
V	65	35	11 0101	01 0101	0	5
W	66	36	11 0110	01 0110	0	6
X	67	37	11 0111	01 0111	0	7
Y	70	38	11 1000	01 1000	0	8
Z	71	39	11 1001	01 1001	0	9
,	72	3A	11 1010	01 1011	0	8-3
%	73	3B	11 1011	01 1100	0	8-4
≠	74	3C	11 1100	01 1010	0	8-2
=	75	3D	11 1101	01 1101	0	8-5
]	76	3E	11 1110	01 1110	0	8-6
"	77	3F	11 1111	01 1111	0	8-7

LOW ▲

▼ HIGH

COLLATING SEQUENCE - USASCII X3.4-1968

USASCII Character	Hex Code	Internal Code
NUL	00	0000 0000
SOH	01	0000 0001
STX	02	0000 0010
ETX	03	0000 0011
EOT	04	0000 0100
ENQ	05	0000 0101
ACK	06	0000 0110
BEL	07	0000 0111
BS	08	0000 1000
HT	09	0000 1001
LF	0A	0000 1010
VT	0B	0000 1011
FF	0C	0000 1100
CR	0D	0000 1101
SO	0E	0000 1110
SI	0F	0000 1111
DLE	10	0001 0000
DC1	11	0001 0001
DC2	12	0001 0010
DC3	13	0001 0011
DC4	14	0001 0100
NAK	15	0001 0101
SYN	16	0001 0110
ETB	17	0001 0111
CAN	18	0001 1000
EM	19	0001 1001
SUB	1A	0001 1010
ESC	1B	0001 1011
FS	1C	0001 1100
GS	1D	0001 1101
RS	1E	0001 1110
US	1F	0001 1111
SP	20	0010 0000
! (or)	21	0010 0001
"	22	0010 0010
#	23	0010 0011
$	24	0010 0100
%	25	0010 0101
&	26	0010 0110
'	27	0010 0111
(	28	0010 1000
)	29	0010 1001
*	2A	0010 1010
+	2B	0010 1011
,	2C	0010 1100
-	2D	0010 1101
.	2E	0010 1110
/	2F	0010 1111
0	30	0011 0000
1	31	0011 0001
2	32	0011 0010
3	33	0011 0011
4	34	0011 0100
5	35	0011 0101
6	36	0011 0110
7	37	0011 0111
8	38	0011 1000
9	39	0011 1001
:	3A	0011 1010
;	3B	0011 1011
<	3C	0011 1100
=	3D	0011 1101
>	3E	0011 1110
?	3F	0011 1111
@	40	0100 0000
A	41	0100 0001
B	42	0100 0010
C	43	0100 0011
D	44	0100 0100
E	45	0100 0101
F	46	0100 0110
G	47	0100 0111
H	48	0100 1000
I	49	0100 1001
J	4A	0100 1010
K	4B	0100 1011
L	4C	0100 1100
M	4D	0100 1101
N	4E	0100 1110
O	4F	0100 1111
P	50	0101 0000
Q	51	0101 0001
R	52	0101 0010
S	53	0101 0011
T	54	0101 0100
U	55	0101 0101
V	56	0101 0110
W	57	0101 0111
X	58	0101 1000

LOW ▲ ▼ HIGH

LOW ▲ ▼ HIGH

COLLATING SEQUENCE - USASCII X3.4-1968 (Cont)

USASCII Character	Hex Code	Internal Code
Y	59	0101 1001
Z	5A	0101 1010
[	5B	0101 1011
\	5C	0101 1100
]	5D	0101 1101
^ (↑)	5E	0101 1100
-	5F	0101 1111
`	60	0110 0000
a	61	0110 0001
b	62	0110 0010
c	63	0110 0011
d	64	0110 0100
e	65	0110 0101
f	66	0110 0110
g	67	0110 0111
h	68	0110 1000
i	69	0110 1001
j	6A	0110 1010
k	6B	0110 1011
l	6C	0110 1100

LOW ▲ ▼ HIGH

USASCII Character	Hex Code	Internal Code
m	6D	0110 1101
n	6E	0110 1110
o	6F	0110 1111
p	70	0111 0000
q	71	0111 0001
r	72	0111 0010
s	73	0111 0011
t	74	0111 0100
u	75	0111 0101
v	76	0111 0110
w	77	0111 0111
x	78	0111 1000
y	79	0111 1001
z	7A	0111 1010
{	7B	0111 1011
|	7C	0111 1100
}	7D	0111 1101
~	7E	0111 1110
DEL	7F	0111 1111

LOW ▲ ▼ HIGH

COLLATING SEQUENCE - BCL TRANSLATED TO EBCDIC

BCL Character	BCL External BA 4321	BCL Hex.	BCL Octal	Translated EBCDIC Code	EBCDIC Hex	Card Code Zone	Card Code Number
(Blank)	01 0000	10	20	0100 0000	40	-	-
[	11 1100	3C	74	0100 1010	4A	12	8-4
.	11 1011	3B	73	0100 1011	4B	12	8-3
<	11 1110	3E	76	0100 1100	4C	12	8-6
(	11 1101	3D	75	0100 1101	4D	12	8-5
+	11 1010	3A	72	0100 1110	4E	12	0
←	11 1111	3F	77	0100 1111	4F	12	8-7
&	11 0000	30	60	0101 0000	50	12	-
]	01 1110	1E	36	0101 1010	5A	0	8-6
$	10 1011	2B	53	0101 1011	5B	11	8-3
*	10 1100	2C	54	0101 1100	5C	11	8-4
)	10 1101	2D	55	0101 1101	5D	11	8-5
;	10 1110	2E	56	0101 1110	5E	11	8-6
≤	10 1111	2F	57	0101 1111	5F	11	8-7
-	10 0000	20	40	0110 0000	60	11	-
/	01 0001	11	21	0110 0001	61	0	1
,	01 1011	1B	33	0110 1011	6B	0	8-3
%	01 1100	1C	34	0110 1100	6C	0	8-4
≠	01 1010	1A	32	0110 1101	6D	0	8-2
>	00 1110	0E	16	0110 1110	6E	-	8-6
?	00 0000	00	00	0110 1111	6F	All other card codes	
:	00 1101	0D	15	0111 1010	7A	-	8-5
#	00 1011	0B	13	0111 1011	7B	-	8-3
@	00 1100	0C	14	0111 1100	7C	-	8-4
≥	00 1111	0F	17	0111 1101	7D	-	8-7
=	01 1101	1D	35	0111 1110	7E	0	8-5
"	01 1111	1F	37	0111 1111	7F	0	8-7
A	11 0001	31	61	1100 0001	C1	12	1
B	11 0010	32	62	1100 0010	C2	12	2
C	11 0011	33	63	1100 0011	C3	12	3
D	11 0100	34	64	1100 0100	C4	12	4
E	11 0101	35	65	1100 0101	C5	12	5
F	11 0110	36	66	1100 0110	C6	12	6
G	11 0111	37	67	1100 0111	C7	12	7
H	11 1000	38	70	1100 1000	C8	12	8
I	11 1001	39	71	1100 1001	C9	12	9

LOW ▲ ▼ HIGH

COLLATING SEQUENCE - BCL TRANSLATED TO EBCDIC (Cont)

BCL Character	BCL External BA 4321	BCL Hex.	BCL Octal	Translated EBCDIC Code	EBCDIC Hex.	Card Zone	Card Number
x(mult)	10 1010	2A	52	1101 0000	D0	11	0
J	10 0001	21	41	1101 0001	D1	11	1
K	10 0010	22	42	1101 0010	D2	11	2
L	10 0011	23	43	1101 0011	D3	11	3
M	10 0100	24	44	1101 0100	D4	11	4
N	10 0101	25	45	1101 0101	D5	11	5
O	10 0110	26	46	1101 0110	D6	11	6
P	10 0111	27	47	1101 0111	D7	11	7
Q	10 1000	28	50	1101 1000	D8	11	8
R	10 1001	29	51	1101 1001	D9	11	9
S	01 0010	12	22	1110 0010	E2	0	2
T	01 0011	13	23	1110 0011	E3	0	3
U	01 0100	14	24	1110 0100	E4	0	4
V	01 0101	15	25	1110 0101	E5	0	5
W	01 0110	16	26	1110 0110	E6	0	6
X	01 0111	17	27	1110 0111	E7	0	7
Y	01 1000	18	30	1110 1000	E8	0	8
Z	01 1001	19	31	1110 1001	E9	0	9
0	00 1010	0A	12	1111 0000	F0	-	0
1	00 0001	01	01	1111 0001	F1	-	1
2	00 0010	02	02	1111 0010	F2	-	2
3	00 0011	03	03	1111 0011	F3	-	3
4	00 0100	04	04	1111 0100	F4	-	4
5	00 0101	05	05	1111 0101	F5	-	5
6	00 0110	06	06	1111 0110	F6	-	6
7	00 0111	07	07	1111 0111	F7	-	7
8	00 1000	08	10	1111 1000	F8	-	8
9	00 1001	09	11	1111 1001	F9	-	9

LOW

HIGH

COLLATING SEQUENCE - BCL TRANSLATED TO USASCII

BCL Character	BCL External BA 8421	BCL Hex.	BCL Octal	Translated USASCII Code	USASCII Hex.	Card Code Zone	Numbers
Blank	01 0000	10	20	0010 0000	20	-	-
←	11 1111	3F	77	0010 0001	21	12	8-7
"	01 1111	1F	37	0010 0010	22	0	8-7
#	01 1011	0B	33	0010 0011	23	-	8-3
$	10 1011	2B	53	0010 0100	24	11	8-3
%	01 1100	1C	34	0010 0101	25	0	8-4
&	11 0000	30	60	0010 0110	26	12	-
≥	01 1111	0F	37	0010 0111	27	-	8-7
(	11 1101	3D	75	0010 1000	28	12	8-3
)	10 1101	2D	55	0010 1001	29	11	8-5
*	10 1100	2C	54	0010 1010	2A	11	8-4
+	11 1010	3A	72	0010 1011	2B	12	0
,	01 1011	1B	33	0010 1100	2C	0	8-3
-	10 0000	20	40	0010 1101	2D	11	-
.	10 1011	3B	53	0010 1110	2E	12	8-3
/	01 0001	11	21	0010 1111	2F	0	1
0	00 1010	0A	12	0011 0000	30	-	0
1	00 0001	01	01	0011 0001	31	-	1
2	00 0010	02	02	0011 0010	32	-	2
3	00 0011	03	03	0011 0011	33	-	3
4	00 0100	04	04	0011 0100	34	-	4
5	00 0101	05	05	0011 0101	35	-	5
6	00 0110	06	06	0011 0110	36	-	6
7	00 0111	07	07	0011 0111	37	-	7
8	00 1000	08	08	0011 1000	38	-	8
9	00 1001	09	09	0011 1001	39	-	9
:	10 1101	0D	55	0011 1010	3A	-	8-5
;	10 1110	2E	56	0011 1011	3B	11	8-6
<	11 1110	3E	76	0011 1100	3C	12	8-6
=	01 1101	1D	35	0011 1101	3D	0	8-5
>	00 1110	0E	16	0011 1110	3E	-	8-6
?	00 0000	00	00	0011 1111	3F	All other card codes	
@	00 1100	0C	14	0100 0000	40	-	8-4
A	11 0001	31	61	0100 0001	41	12	1
B	11 0010	32	62	0100 0010	42	12	2
C	11 0011	33	63	0100 0011	43	12	3
D	11 0100	34	64	0100 0100	44	12	4
E	11 0101	35	65	0100 0101	45	12	5
F	11 0110	36	66	0100 0110	46	12	6
G	11 0111	37	67	0100 0111	47	12	7
H	11 1000	38	70	0100 1000	48	12	8
I	11 1001	39	71	0100 1001	49	12	9
J	10 0001	21	41	0100 1010	4A	11	1
K	10 0010	22	42	0100 1011	4B	11	2
L	10 0011	23	43	0100 1100	4C	11	3

LOW ▲ ▼ HIGH

COLLATING SEQUENCE - BCL TRANSLATED TO USASCII (Cont)

BCL Character	BCL External BA 8421	BCL Hex.	BCL Octal	Translated USASCII Code	USASCII Hex.	Card Code Zone	Card Code Number
M	10 0100	24	44	0100 1101	4D	11	4
N	10 0101	25	45	0100 1110	4E	11	5
O	10 0110	26	46	0100 1111	4F	11	6
P	10 0111	27	47	0101 0000	50	11	7
Q	10 1000	28	50	0101 0001	51	11	8
R	10 1001	29	51	0101 0010	52	11	9
S	01 0010	12	22	0101 0011	53	0	2
T	01 0011	13	23	0101 0100	54	0	3
U	01 0100	14	24	0101 0101	55	0	4
V	01 0101	15	25	0101 0110	56	0	5
W	01 0110	16	26	0101 0111	57	0	6
X	01 0111	17	27	0101 1000	58	0	7
Y	01 1000	18	30	0101 1001	59	0	8
Z	01 1001	19	31	0101 1010	5A	0	9
[	11 1100	3C	74	0101 1011	5B	12	8-4
]	01 1110	1E	36	0101 1101	5D	0	8-6
<	10 1111	2F	57	0101 1110	5E	11	8-7
≠	01 1010	1A	32	0101 1111	5F	0	8-2
x(Mult)	10 1010	2A	52	0111 1101	7D	11	0

LOW ▲ ▼ HIGH

COLLATING SEQUENCE - USASCII X3.4-1968 TRANSLATED TO EBCDIC

USASCII Character	USASCII Hex. Code	Translated EBCDIC Code	EBCDIC Hex. Code
NULL	00	0000 0000	00
SOH	01	0000 0001	01
STX	02	0000 0010	02
ETX	03	0000 0011	03
HT	09	0000 0101	05
DEL	7F	0000 0111	07
VT	0B	0000 1011	0B
FF	0C	0000 1100	0C
CR	0D	0000 1101	0D
SO	0E	0000 1110	0E
SI	0F	0000 1111	0F
DLE	10	0001 0000	10
DC1	11	0001 0001	11
DC2	12	0001 0010	12
DC3	13	0001 0011	13
BS	08	0001 0110	16
CAN	18	0001 1000	18
EM	19	0001 1001	19
FS	1C	0001 1100	1C
GS	1D	0001 1101	1D
RS	1E	0001 1110	1E
US	1F	0001 1111	1F
LF	0A	0010 0101	25
ETB	17	0010 0110	26
ESC	1B	0010 0111	27
ENQ	05	0010 1101	2D
ACK	06	0010 1110	2E
BEL	07	0010 1111	2F
SYN	16	0011 0010	32
EOT	04	0011 0111	37
DC4	14	0011 1100	3C
NAK	15	0011 1101	3D
SUB	1A	0011 1111	3F
SP	20	0100 0000	40
[	5B	0100 1010	4A
.	2E	0100 1011	4B
<	3C	0100 1100	4C
(	28	0100 1101	4D
+	2B	0100 1110	4E
| (or)	21	0100 1111	4F

LOW ▲ ▼ HIGH

COLLATING SEQUENCE - USASCII X3.4-1968 TRANSLATED TO EBCDIC (Cont)

USASCII Character	USASCII Hex. Code	Translated EBCDIC Code	EBCDIC Hex. Code
&	26	0101 0000	50
]	5D	0101 1010	5A
$	24	0101 1011	5B
*	2A	0101 1100	5C
)	29	0101 1101	5D
;	3B	0101 1110	5E
^ (¬)	5E	0101 1111	5F
-	2D	0110 0000	60
/	2F	0110 0001	61
¦	7C	0110 1010	6A
,	2C	0110 1011	6B
%	25	0110 1100	6C
_	5F	0110 1101	6D
>	3E	0110 1110	6E
?	3F	0110 1111	6F
`	60	0111 1001	79
:	3A	0111 1010	7A
#	23	0111 1011	7B
@	40	0111 1100	7C
'	27	0111 1101	7D
=	3D	0111 1110	7E
"	22	0111 1111	7F
a	61	1000 0001	81
b	62	1000 0010	82
c	63	1000 0011	83
d	64	1000 0100	84
e	65	1000 0101	85
f	66	1000 0110	86
g	67	1000 0111	87
h	68	1000 1000	88
i	69	1000 1001	89
j	6A	1001 0001	91
k	6B	1001 0010	92
l	6C	1001 0011	93
m	6D	1001 0100	94
n	6E	1001 0101	95
o	6F	1001 0110	96
p	70	1001 0111	97
q	71	1001 1000	98
r	72	1001 1001	99
~	7D	1010 0001	A1
s	73	1010 0010	A2

LOW ▲ ▼ HIGH

COLLATING SEQUENCE - USASCII X3.4-1968 TRANSLATED TO EBCDIC (Cont)

USASCII Character	USASCII Hex. Code	Translated EBCDIC Code	EBCDIC Hex. Code
t	74	1010 0011	A3
u	75	1010 0100	A4
v	76	1010 0101	A5
w	77	1010 0110	A6
x	78	1010 0111	A7
y	79	1010 1000	A8
z	7A	1010 1001	A9
{	7B	1100 0000	C0
A	41	1100 0001	C1
B	42	1100 0010	C2
C	43	1100 0011	C3
D	44	1100 0100	C4
E	45	1100 0101	C5
F	46	1100 0110	C6
G	47	1100 0111	C7
H	48	1100 1000	C8
I	49	1100 1000	C9
}	70	1101 0000	D0
J	4A	1101 0001	D1
K	4B	1101 0010	D2
L	4C	1101 0011	D3
M	4D	1101 0100	D4
N	4E	1101 0101	D5
O	4F	1101 0110	D6
P	50	1101 0111	D7
Q	51	1101 1000	D8
R	52	1101 1001	D9
\	5C	1110 0000	E0
S	53	1110 0010	E2
T	54	1110 0011	E3
U	55	1110 0100	E4
V	56	1110 0101	E5
W	57	1110 0110	E6
X	58	1110 0111	E7
Y	59	1110 1000	E8
Z	5A	1110 1001	E9



COLLATING SEQUENCE - USASCII X3.4-1968 TRANSLATED TO EBCDIC (Cont)

USASCII Character	USASCII Hex. Code	Translated EBCDIC Code	EBCDIC Hex. Code
0	30	1111 0000	F0
1	13	1111 0001	F1
2	32	1111 0010	F2
3	33	1111 0011	F2
4	34	1111 0100	F4
5	35	1111 0101	F5
6	36	1111 0110	F6
7	37	1111 0111	F7
8	38	1111 1000	F8
9	39	1111 1001	F9

LOW
HIGH

XALGOL COLLATING SEQUENCE (B 5700 BCL)

BCL Character	BCL Octal	BCL Hex	BCL Internal BA 8421	BCL External BA 8421	Card Code Zone	Card Code Number
Blank	60	30	11 0000	01 0000	-	-
.	32	1A	01 1010	11 1011	12	8-3
[	33	1B	01 1011	11 1100	12	8-4
(	35	1D	01 1101	11 1101	12	8-5
<	36	1E	01 1110	11 1110	12	8-6
+	37	1F	01 1111	11 1111	12	8-7
&	34	1C	01 1100	11 0000	12	-
$	52	2A	10 1010	10 1011	11	8-3
*	53	2B	10 1011	10 1100	11	8-4
)	55	2D	10 1101	10 1101	11	8-5
;	56	2E	10 1110	10 1110	11	8-6
≤	57	2F	10 1111	10 1111	11	8-7
-	54	2C	10 1100	10 0000	11	-
/	61	31	11 0001	01 0001	0	1
,	72	3A	11 1010	01 1011	0	8-3
%	73	3B	11 1011	01 1100	0	8-4
=	75	3D	11 1101	01 1101	0	8-5
]	76	3E	11 1110	01 1110	0	8-6
"	77	3F	11 1111	01 1111	0	8-7
#	12	0A	00 1010	00 1011	-	8-3
@	13	0B	00 1011	00 1100	-	8-4
:	15	0D	00 1101	00 1101	-	8-5
>	16	0E	00 1110	00 1110	-	8-6
≥	17	0F	00 1111	00 1111	-	8-7
+	20	10	01 0000	11 1010	12	0
A	21	11	01 0001	11 0001	12	1
B	22	12	01 0010	11 0010	12	2
C	23	13	01 0011	11 0011	12	3
D	24	14	01 0100	11 0100	12	4
E	25	15	01 0101	11 0101	12	5
F	26	16	01 0110	11 0110	12	6
G	27	17	01 0111	11 0111	12	7
H	30	18	01 1000	11 1000	12	8
I	31	19	01 1001	11 1001	12	9
x	40	20	10 0000	10 1010	11	0
J	41	21	10 0001	10 0001	11	1
K	42	22	10 0010	10 0010	11	2
L	43	23	10 0011	10 0011	11	3
M	44	24	10 0100	10 0100	11	4
N	45	25	10 0101	10 0101	11	5

LOW ↑ COLLATING SEQUENCE ↓ HIGH

XALGOL COLLATING SEQUENCE (Cont)
(B 5700 BCL)

BCL Character	BCL Octal	BCL Hex	BCL Internal BA 8421	BCL External BA 8421	Card Code Zone Number	
0	46	26	10 0110	10 0110	11 6	
P	47	27	10 0111	10 0111	11 7	LOW
Q	50	28	10 1000	10 1000	11 8	↑
R	51	29	10 1001	10 1001	11 9	↓
≠	74	3C	11 1100	01 1010	0 8-2	
S	62	32	11 0010	01 0010	0 2	
T	63	33	11 0011	01 0011	0 3	
U	64	34	11 0100	01 0100	0 4	
V	65	35	11 0101	01 0101	0 5	
W	66	36	11 0110	01 0110	0 6	
X	67	37	11 0111	01 0111	0 7	
Y	70	38	11 1000	01 1000	0 8	
Z	71	39	11 1001	01 1001	0 9	
0	00	00	00 0000	00 1010	- 0	
1	01	01	00 0001	00 0001	- 1	HIGH
2	02	02	00 0010	00 0010	- 2	
3	03	03	00 0011	00 0011	- 3	
4	04	04	00 0100	00 0100	- 4	
5	05	05	00 0101	00 0101	- 5	
6	06	06	00 0110	00 0110	- 6	
7	07	07	00 0111	00 0111	- 7	
8	10	08	00 1000	00 1000	- 8	
9	11	09	00 1001	00 1001	- 9	
?	14	0C	00 1100	00 0000	ALL OTHER CARD CODES	

FORTRAN BCD COLLATING SEQUENCE

BCD Character	Internal Representation Hex	Internal Representation Binary	Internal Translation Binary	Internal Translation Hex	Card Code Zone	Card Code Number
. (period)	1A	01 1010	0100 1011	4B	12	8-3
)	1B	01 1011	0100 1100	4C	12	8-4
+	1C	01 1100	0101 0000	50	12	
$	2A	10 1010	0101 1011	5B	11	8-3
*	2B	10 1011	0101 1100	5C	11	8-4
;	2E	10 1110	0101 1110	5E	11	8-6
≤	2F	10 1111	0101 1111	5F	11	8-7
- (minus)	2C	10 1100	0110 0000	60	11	
/	31	11 0001	0110 0001	61	0	1
, (comma)	3A	11 1010	0110 1011	6B	0	8-3
(	3B	11 1011	0110 1100	6C	0	8-4
≠	3D	11 1101	0110 1101	6D	0	8-5
>	3E	11 1110	0110 1110	6E	0	8-6
?	3F	11 1111	0110 1111	6F	0	8-7
=	0A	00 1010	0111 1011	7B		8-3
@	0B	00 1011	0111 1100	7C		8-4
≥	0D	00 1101	0111 1101	7D		8-5
≠	0E	00 1110	0111 1110	7E		8-6
"	0F	00 1111	0111 1111	7E		8-7
A	11	01 0001	1100 0001	C1	12	1
B	12	01 0010	1100 0010	C2	12	2
C	13	01 0011	1100 0011	C3	12	3
D	14	01 0100	1100 0100	C4	12	4
E	15	01 0101	1100 0101	C5	12	5
F	16	01 0110	1100 0110	C6	12	6
G	17	01 0111	1100 0111	C7	12	7
H	18	01 1000	1100 1000	C8	12	8
I	19	01 1001	1100 1001	C9	12	9
J	21	10 0001	1101 0001	D1	11	1
K	22	10 0010	1101 0010	D2	11	2
L	23	10 0011	1101 0011	D3	11	3
M	24	10 0100	1101 0100	D4	11	4
N	25	10 0101	1100 0101	D5	11	5
O	26	10 0110	1101 0110	D6	11	6
P	27	10 0111	1101 0111	D7	11	7
Q	28	10 1000	1101 1000	D8	11	8
R	29	10 1001	1101 1001	D9	11	9
S	31	11 0010	1110 0010	E2	0	2
T	33	11 0011	1110 0011	E3	0	3
U	34	11 0100	1110 0100	E4	0	4
V	35	11 0101	1110 0101	E5	0	5
W	36	11 0110	1110 0110	E6	0	6
X	37	11 0111	1110 0111	E7	0	7
Y	38	11 1000	1110 1000	E8	0	8
Z	39	11 1001	1110 1001	E9	0	9
0	00	00 0000	1111 0000	F0		0
1	01	00 0001	1111 0001	F1		1
2	02	00 0010	1111 0010	F2		2

Low ↑ ↓ High

FORTRAN BCD COLLATING SEQUENCE (Cont)

BCD Character	Internal Representation		Internal Translation		Card Code Zone Number
	Hex	Binary	Binary	Hex	
3	03	00 0011	1111 0011	F3	3
4	04	00 0100	1111 0100	F4	4
5	05	05 0101	1111 0101	F5	5
6	06	00 0110	1111 0110	F6	6
7	07	00 0111	1111 0111	F7	7
8	08	00 1000	1111 1000	F8	8
9	09	00 1001	1111 1001	F9	9

Low

High

EXTENDED BINARY CODED DECIMAL INTERCHANGE CODES (EBCDIC)

b4 b3 b2 b1	ROW \ COL	0 (0 0 0 0)	1 (0 0 0 1)	2 (0 0 1 0)	3 (0 0 1 1)	4 (0 1 0 0)	5 (0 1 0 1)	6 (0 1 1 0)	7 (0 1 1 1)	8 (1 0 0 0)	9 (1 0 0 1)	10 (A) (1 0 1 0)	11 (B) (1 0 1 1)	12 (C) (1 1 0 0)	13 (D) (1 1 0 1)	14 (E) (1 1 1 0)	15 (F) (1 1 1 1)
0 0 0 0	0	NUL 12-0-9-8-1	DLE 12-11-9-8-1	11-0-9-8-1	12-11-0-9-8-1	SP BLANK	& 12	- 11		12-0-8-1		11-0-8-1	12-11-0-8-1	PZ(+) 12-0	MZ (-) 11-0	\(CR)(t) 0-8-2	0
0 0 0 1	1	SOH 12-9-1	DC1 11-9-1	0-9-1	9-1	12-0-9-1	12-11-9-1	/ 0-1		a 12-0-1	J 12-11-1	11-0-1	12-11-0-1	A 12-1	J 11-1	11-0-8-1	1
0 0 1 0	2	STX 12-9-2	DC2 11-9-2	0-9-2	SYN 9-2	12-0-9-2	12-11-9-2	11-0-9-2	12-11-0-9-2	b 12-0-2	K 12-11-2	s 11-0-2	12-11-0-2	B 12-2	K 11-2	S 0-2	2
0 0 1 1	3	ETX 12-9-3	DC3 11-9-3	0-9-3	9,3	12-0-9-3	12-11-9-3	t 11-0-9-3	12-11-0-9-3	c 12-0-3	L 12-11-3	t 11-0-3	12-11-0-3	C 12-3	L 11,3	T 0-5	3
0 1 0 0	4	12-9-4	11-9-4	0-9-4	9-4	12-0-9-4	12-11-9-4	11-0-9-4	12-11-0-9-4	d 12-0-4	M 12-11-4	u 11-0-4	12-11-0-4	D 12-4	M 11-4	U 0-4	4
0 1 0 1	5	HT 12-9-5	NL 11-9-5	LF 0-9-5	9-5	12-0-9-5	12-11-9-5	11-0-9-5	12-11-0-9-5	e 12-0-5	n 12-11-5	v 11-0-5	12-11-0-5	E 12-5	N 11-5	V 0-5	5
0 1 1 0	6	12-9-6	BS 11-9-6	ETB 0-9-6	9-6	12-0-9-6	12-11-9-6	11-0-9-6	12-11-0-9-6	f 12-0-6	o 12-11-6	w 11-0-6	12-11-0-6	F 12-6	O 11-6	W 0-6	6
0 1 1 1	7	DEL 12-9-7	11-9-7	ESC 0-9-7	EOT 9-7	12-0-9-7	12-11-9-7	11-0-9-7	12-11-0-9-7	g 12-0-7	p 12-11-7	x 11-0-7	12-11-0-7	G 12-7	P 11-7	X 0-7	7
1 0 0 0	8	12-9-8	CAN 11-9-8	0-9-8	9-8	12-0-9-8	12-11-9-8	11-0-9-8	12-11-0-9-8	h 12-0-8	q 12-11-8	y 11-0-8	12-11-0-8	H 12-8	Q 11-8	Y 0-8	8
1 0 0 1	9	12-9-8-1	EM 11-9-8-1	0-9-8-1	9-8-1	12-8-1	11-8-1	0-8-1	8-1	i 12-0-9	r 12-11-9	z 11-0-9	12-11-0-9	I 12-9	R 11-9	Z 0-9	9
1 0 1 0	10 (A)	12-9-8-2	11-9-8-2	0-9-8-2	9-8-2	12-8-2	11-8-2	12-11	8-2	12-0-8-2	12-11-0-8-2	11-0-8-2	12-11-0-8-2	12-0-9-8-2	12-11-9-8-2	11-0-9-8-2	12-11-0-9-8-2
1 0 1 1	11 (B)	VT 12-9-8-3	11-9-8-3	0-9-8-3	9-8-3	12-8-3	11-8-3	0-8-3	# 8-3	12-0-8-3	12-11-0-8-3	11-0-8-3	12-11-0-8-3	12-0-9-8-3	12-11-9-8-3	11-0-9-8-3	12-11-0-9-8-3
1 1 0 0	12 (C)	FF 12-9-8-4	FS 11-9-8-4	0-9-8-4	DC4 9-8-4	< 12-8-4	* 11-8-4	% 0-8-4	@ 8-4	12-0-8-4	12-11-8-4	11-0-8-4	12-11-0-8-4	12-0-9-8-4	12-11-9-8-4	11-0-9-8-4	12-11-0-9-8-4
1 1 0 1	13 (D)	CR 12-9-8-5	GS 11-9-8-5	ENQ 0-9-8-5	NAK 9-8-5	(12-8-5	) 11-8-5	(US)(≠) 0-8-5	¢(≥) 8-5	12-0-8-5	12-11-8-5	11-0-8-5	12-11-0-8-5	12-0-9-8-5	12-11-9-8-5	11-0-9-8-5	12-11-0-9-8-5
1 1 1 0	14 (E)	SO 12-9-8-6	RS 11-9-8-6	ACK 0-9-8-6	9-8-6	+ 12-8-6	; 11-8-6	>= 0-8-6	= 8-6	12-0-8-6	12-11-8-6	11-0-8-6	12-11-0-8-6	12-0-9-8-6	12-11-9-8-6	11-0-9-8-6	12-11-0-9-8-6
1 1 1 1	15 (F)	SI 12-9-8-7	US 11-9-8-7	BEL 0-9-8-7	SUB 9-8-7	|(←)* 12-8-7	¬(≤) 11-8-7	? 0-8-7	# 8-7	12-0-8-7	12-11-8-7	11-0-8-7	DELIMETER 12-11-0-8-7	12-0-9-8-7	12-11-9-8-7	11-0-9-8-7	12-11-0-9-8-7

$b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1$

*INTERNAL COLLATING SEQUENCE - 0 0 0 0 0/0 0 0 0 TO 1111/1111

APPENDIX F
DATA REPRESENTATION

EBCDIC GRAPHIC	BCL	DECIMAL VALUE	EBCDIC INTERNAL	HEX. GRAPHIC	EBCDIC CARD CODE	BCL CARD CODE	OCTAL	BCL INTERNAL	BCL EXTERNAL
BLANK		64	0100 0000	40	No Punches	No Punches	60	11 0000	01 0000
[		74	0100 1010	4A	12 8 2	12 8 4	33	01 1011	11 1100
.		75	0100 1011	4B	12 8 3	12 8 3	32	01 1010	11 1011
<		76	0100 1100	4C	12 8 4	12 8 6	36	01 1110	11 1110
(		77	0100 1101	4D	12 8 5	12 8 5	35	01 1101	11 1101
+		78	0100 1110	4E	12 8 6				11 1010
!	←	79	0100 1111	4F	12 8 7	12 8 7	37	01 1111	11 1111
&		80	0101 0000	50	12	12	34	01 1100	11 0000
]		90	0101 1010	5A	11 8 2	0 8 6	76	11 1110	01 1110
$		91	0101 1011	5B	11 8 3	11 8 3	52	10 1010	10 1011
*		92	0101 1100	5C	11 8 4	11 8 4	53	10 1011	10 1100
)		93	0101 1101	5D	11 8 5	11 8 5	55	10 1101	10 1101
;		94	0101 1110	5E	11 8 6	11 8 6	56	10 1110	10 1110
¬	≤	95	0101 1111	5F	11 8 7	11 8 7	57	10 1111	10 1111
-		96	0110 0000	60	11	11	54	10 1100	10 0000
/		97	0110 0001	61	0 1	0 1	61	11 0001	01 0001
,		107	0110 1011	6B	0 8 3	0 8 3	72	11 1010	01 1011
%		108	0110 1100	6C	0 8 4	0 8 4	73	11 1011	01 1100
_	≠	109	0110 1101	6D	0 8 5	0 8 2	74	11 1100	01 1010
>		110	0110 1110	6E	0 8 6	8 6	16	00 1110	00 1110
?		111	0110 1111	6F	0 8 7	*	14	00 1100	00 0000
:		122	0111 1010	7A	8 2	8 5	15	00 1101	00 1101
#		123	0111 1011	7B	8 3	8 3	12	00 1010	00 1011
@		124	0111 1100	7C	8 4	8 4	13	00 1011	00 1100
'	≥	125	0111 1101	7D	8 5	8 7	17	00 1111	00 1111
=		126	0111 1110	7E	8 6	0 8 5	75	11 1101	01 1101
"		127	0111 1111	7F	8 7	0 8 7	77	11 1111	01 1111
(+)PZ	+	192	1100 0000	CO	12 0	12 0	20	01 0000	11 1010
A		193	1100 0001	C1	12 1	12 1	21	01 0001	11 0001
B		194	1100 0010	C2	12 2	12 2	22	01 0010	11 0010
C		195	1100 0011	C3	12 3	12 3	23	01 0011	11 0011
D		196	1100 0100	C4	12 4	12 4	24	01 0100	11 0100
E		197	1100 0101	C5	12 5	12 5	25	01 0101	11 0101
F		198	1100 0110	C6	12 6	12 6	26	01 0110	11 0110
G		199	1100 0111	C7	12 7	12 7	27	01 0111	11 0111
H		200	1100 1000	C8	12 8	12 8	30	01 1000	11 1000
I		201	1100 1001	C9	12 9	12 9	31	01 1001	11 1001
(!)MZ	MULT x	208	1101 0000	D0	11 0	11 0	40	10 0000	10 1010
J		209	1101 0001	D1	11 1	11 1	41	10 0001	10 0001
K		210	1101 0010	D2	11 2	11 2	42	10 0010	10 0010
L		211	1101 0011	D3	11 3	11 3	43	10 0011	10 0011
M		212	1101 0100	D4	11 4	11 4	44	10 0100	10 0100
N		213	1101 0101	D5	11 5	11 5	45	10 0101	10 0101
O		214	1101 0110	D6	11 6	11 6	46	10 0110	10 0110
P		215	1101 0111	D7	11 7	11 7	47	10 0111	10 0111

*All other codes

DATA REPRESENTATION

EBCDIC GRAPHIC	BCL	DECIMAL VALUE	EBCDIC INTERNAL	HEX. GRAPHIC	EBCDIC CARD CODE	BCL CARD CODE	OCTAL	BCL INTERNAL	BCL EXTERNAL
Q		216	1101 1000	D8	11 8	11 8	50	10 1000	10 1000
R		217	1101 1001	D9	11 9	11 9	51	10 1001	10 1001
¢		224	1110 0000	E0	0 8 2				00 0000
S		226	1110 0010	E2	0 2	0 2	62	11 0010	01 0010
T		227	1110 0011	E3	0 3	0 3	63	11 0011	01 0011
U		228	1110 0100	E4	0 4	0 4	64	11 0100	01 0100
V		229	1110 0101	E5	0 5	0 5	65	11 0101	01 0101
W		230	1110 0110	E6	0 6	0 6	66	11 0110	01 0110
X		231	1110 0111	E7	0 7	0 7	67	11 0111	01 0111
Y		232	1110 1000	E8	0 8	0 8	70	11 1000	01 1000
Z		233	1110 1001	E9	0 9	0 9	71	11 1001	01 1001
0		240	1111 0000	F0	0	0	00	00 0000	00 1010
1		241	1111 0001	F1	1	1	01	00 0001	00 0001
2		242	1111 0010	F2	2	2	02	00 0010	00 0010
3		243	1111 0011	F3	3	3	03	00 0011	00 0011
4		244	1111 0100	F4	4	4	04	00 0100	00 0100
5		245	1111 0101	F5	5	5	05	00 0101	00 0101
6		246	1111 0110	F6	6	6	06	00 0110	00 0110
7		247	1111 0111	F7	7	7	07	00 0111	00 0111
8		248	1111 1000	F8	8	8	10	00 1000	00 1000
9		249	1111 1001	F9	9	9	11	00 1001	00 1001

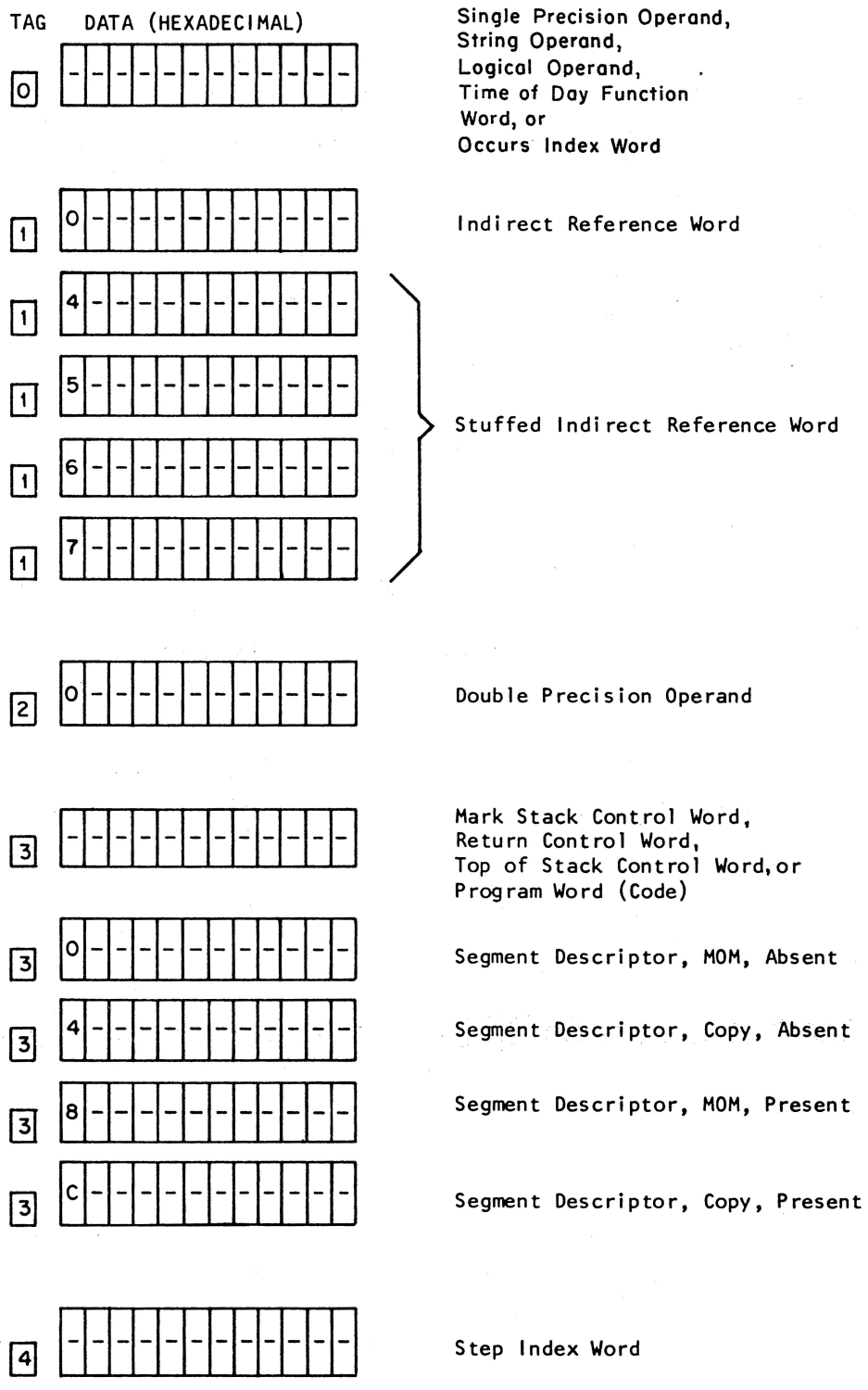
NOTES

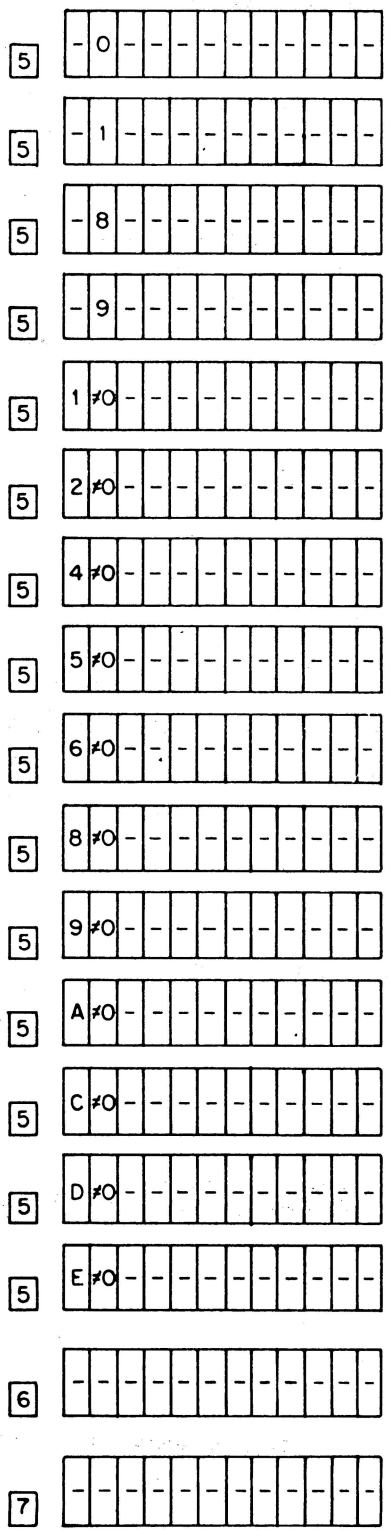
1. EBCDIC 0100 1110 also translates to BCL 11 1010.
2. EBCDIC 1100 1111 is translated to BCL 00 0000 with an additional flag bit on the most significant bit line (8th bit). This function is used by the unbuffered printer to stop scanning.
3. EBCDIC 1110 0000 is translated to BCL 00 0000 with an additional flag bit on the next to most significant bit line (7th bit). As the print drums have 64 graphics and space this signal can be used to print the 64th graphic. The 64th graphic is a "CR" for BCL drums and a "¢" for EBCDIC drums.
4. The remaining 189 EBCDIC codes are translated to BCL 00 0000 (? code).
5. The EBCDIC graphics and BCL graphics are the same except as follows:

BCL		EBCDIC
≥		' (single quote)
x	(multiply)	!
≤		¬ (not)
≠		¯ (underscore)
←		

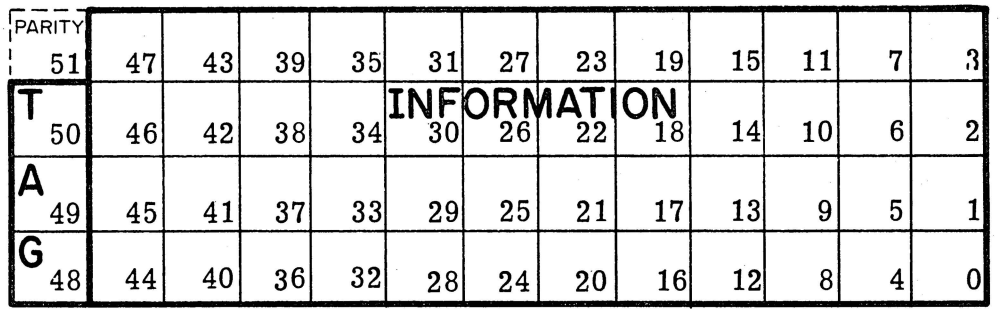
APPENDIX G
WORD FORMATS

WORD IDENTIFICATION




5 - 0 - - - - - - - - - -
Data Descriptor, Single, Read/Write
5 - 1 - - - - - - - - - -
Data Descriptor, Double, Read/Write
5 - 8 - - - - - - - - - -
Data Descriptor, Single, Read-only
5 - 9 - - - - - - - - - -
Data Descriptor, Double, Read-only
5 1 ≠0 - - - - - - - - -
String Descriptor, Non-Indexed
5 2 ≠0 - - - - - - - - -
String Descriptor, Indexed
5 4 ≠0 - - - - - - - - -
String Descriptor, Non-Indexed
5 5 ≠0 - - - - - - - - -
String Descriptor, Non-Indexed
5 6 ≠0 - - - - - - - - -
String Descriptor, Indexed
5 8 ≠0 - - - - - - - - -
String Descriptor, Non-Indexed
5 9 ≠0 - - - - - - - - -
String Descriptor, Non-Indexed
5 A ≠0 - - - - - - - - -
String Descriptor, Indexed
5 C ≠0 - - - - - - - - -
String Descriptor, Non-Indexed
5 D ≠0 - - - - - - - - -
String Descriptor, Non-Indexed
5 E ≠0 - - - - - - - - -
String Descriptor, Indexed
6 - - - - - - - - - - -
Unitialized Operand (Software Usage - Block Exit) or DCP Code
7 - - - - - - - - - - -
Program Control Word

BASIC WORD FORMAT



Field	Bits	Description
Parity	50:1	Parity bit. Odd parity for the 51 bit word.
Tag	50:3	Value of this field indicates the usage of the information field, as described below.

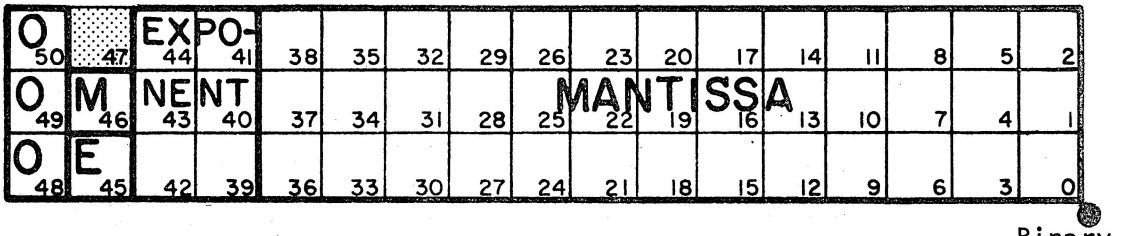
Tag Value	Information Field Usage
0	Single Precision Operand, Logical Operand, String Operand, Occurs Index Word, Time of Day Function Word
1	Indirect Reference Word, Stuffed Indirect Reference Word
2	Double Precision Operand
3	Mark Stack Control Word, Return Control Word, Top of Stack Control Word, Program Word, Segment Descriptor
4	Step Index Word
5	Data Descriptor, String Descriptor
6	Uninitialized Operand
7	Program Control Word

INFORMATION	47:48	Use of this field depends on the value of the tag field.

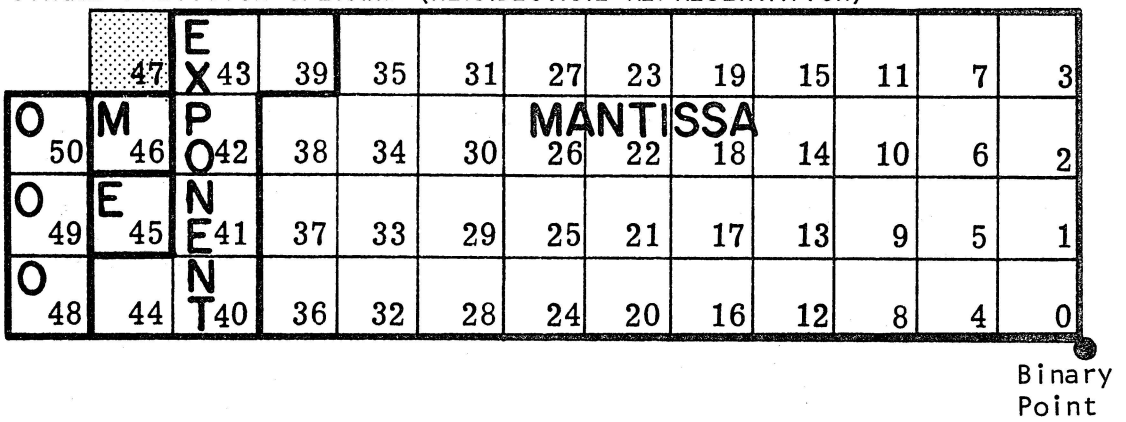
40978

SINGLE PRECISION OPERAND

SINGLE PRECISION OPERAND (OCTAL REPRESENTATION)



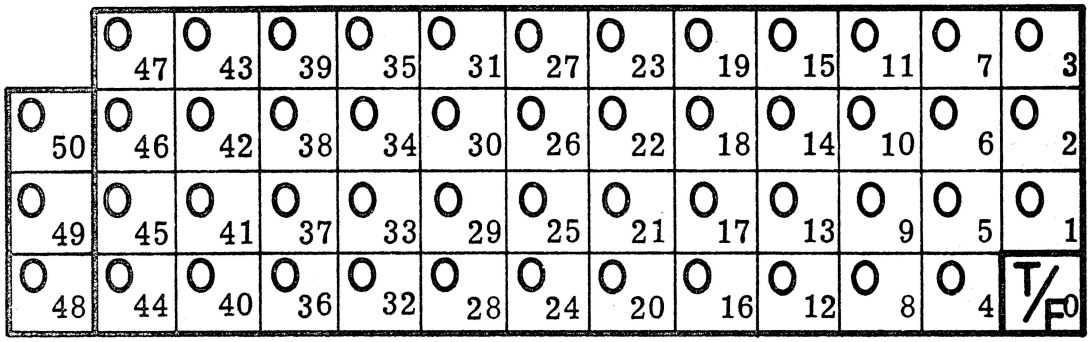
SINGLE PRECISION OPERAND (HEXADECIMAL REPRESENTATION)



TAG	50:13	000
	47:1	Not used
M	46:1	Sign of Mantissa.
		1 = Negative, 0 = Positive.
E	45:1	Sign of exponent.
		1 = Negative, 0 = Positive.
EXPONENT	44:6	Exponent.
MANTISSA	38:39	Mantissa.

40960

LOGICAL OPERAND

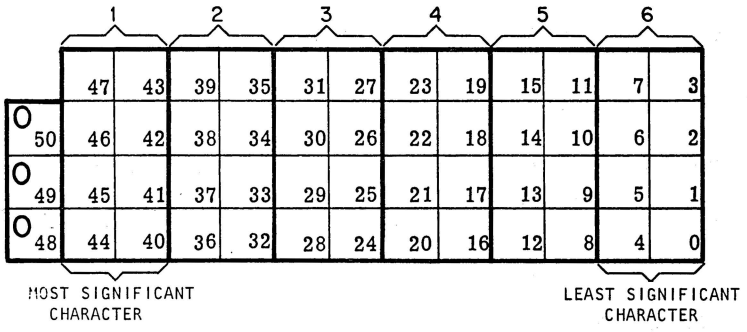


Field	Bits	Description
TAG	50:3	000
	47:47	All zeroes.
T/F	0:1	True/false bit.
		1 = True, 0 = False

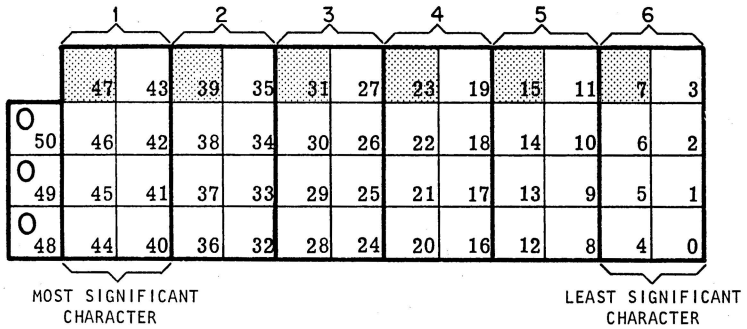
40963

STRING OPERANDS

8-BIT BYTES (EBCDIC CODE)

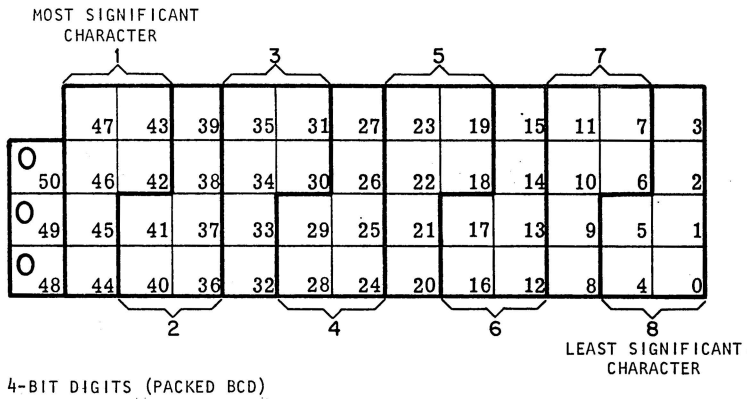


7-BIT CHARACTERS (USASCII CODE)

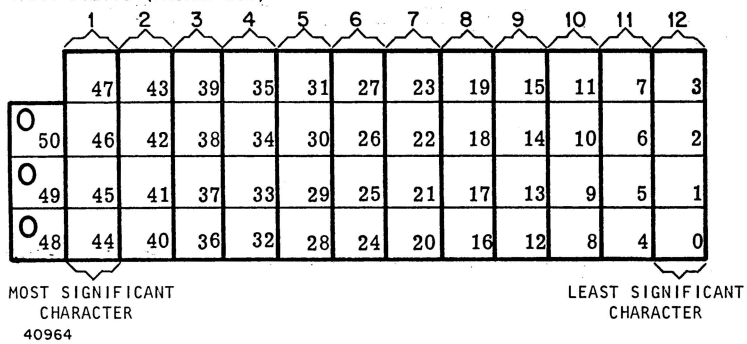


(BITS 47,39,31,23,15,AND 7 ARE NOT USED)

6-BIT CHARACTERS (BCL CODE)



4-BIT DIGITS (PACKED BCD)



40964

STRING OPERANDS (Cont'd)

The sign of a numeric field is represented as follows:

a. 8-bit characters

The sign is in the zone bits of the least significant character (bits 7 thru 4 of the field). A bit configuration of 1101 indicates a negative number; any other bit configuration indicates a positive number.

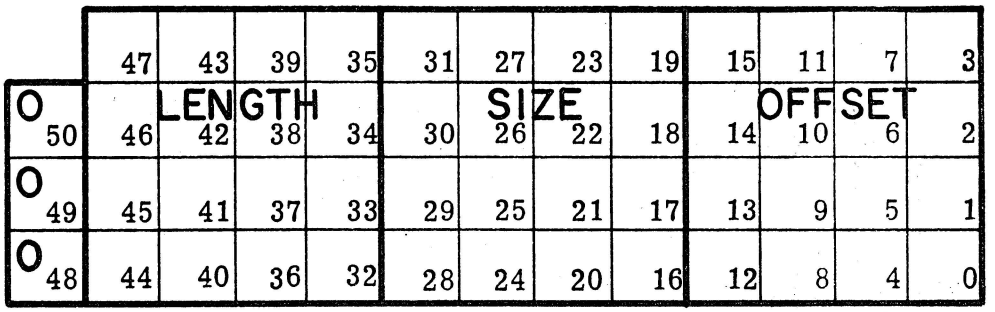
b. 6-bit characters

The sign is in the zone bits of the least significant character (bits 5 and 4 of the field). A bit configuration of 10 indicates a negative number; any other bit configuration indicates a positive number.

c. 4-bit digits

The sign is carried as a separate digit, and it is the most significant digit of the field. A bit configuration of 1101 indicates a negative number; any other bit configuration indicates a positive number.

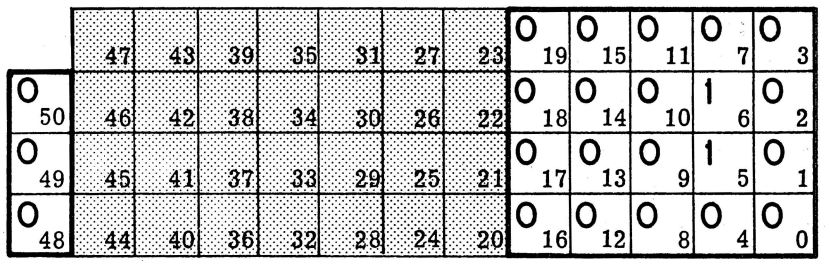
OCCURS INDEX WORD



Field	Bits	Description
Tag	50:3	Tag field. Value equals zero.
LENGTH	47:16	The length, in characters, of each field in the array.
SIZE	31:16	The size, in fields, of the array.
OFFSET	15:16	The number of characters preceding the first field of the array.

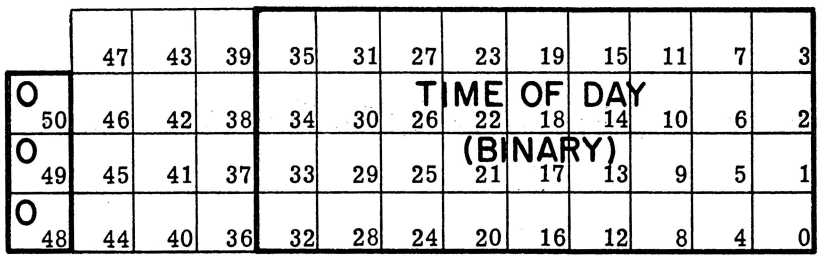
40989

TIME OF DAY FUNCTION WORD



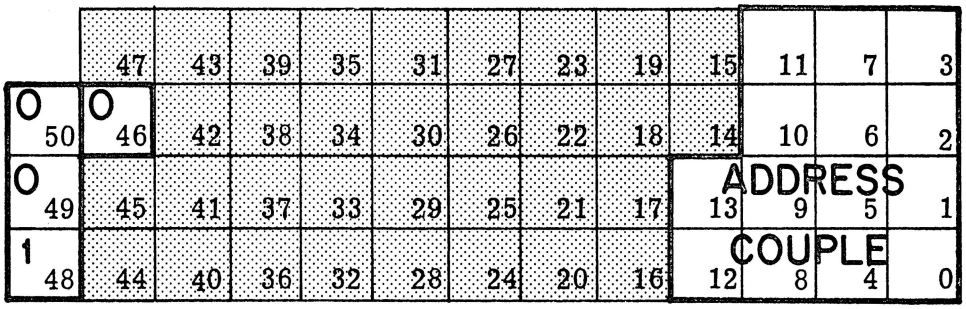
Field	Bits	Description
Tag	50:3	Tag field. Value equal zero.
	47:28	Not used.
	19:13	Must equal zero.
	6:2	Must equal three.
	4:5	Must equal zero.

TIME OF DAY VALUE RETURNED



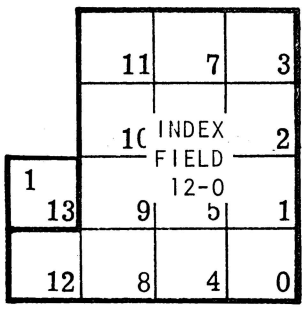
40990

INDIRECT REFERENCE WORD

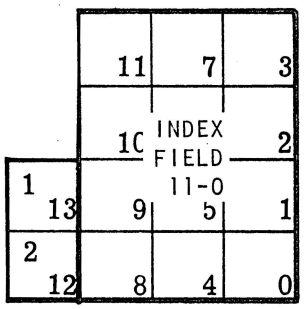


Field	Bits	Description
Tag	50:3	Tag field. Value equals one.
	47:1	Not used
	46:1	Environment bit. Must equal zero for an IRW. (1 = SIRW).
	45:32	Not used.
Address Couple	13:14	SELECTS D REGISTER (ACCORDING TO CURRENT PROGRAM LEVEL AS INDICATED BY rLL) AND PROVIDES INDEX VALUE (SEE BELOW).

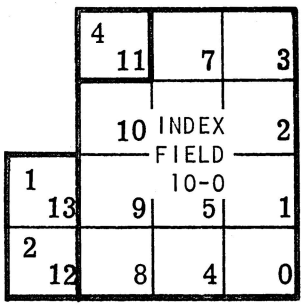
PROGRAM LEVEL 0-1



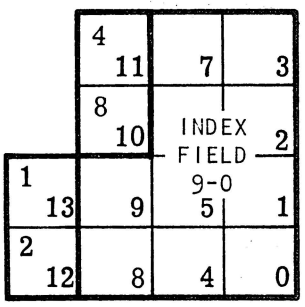
PROGRAM LEVEL 0-3



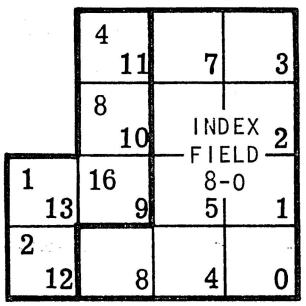
PROGRAM LEVEL 0-7



PROGRAM LEVEL 0-15



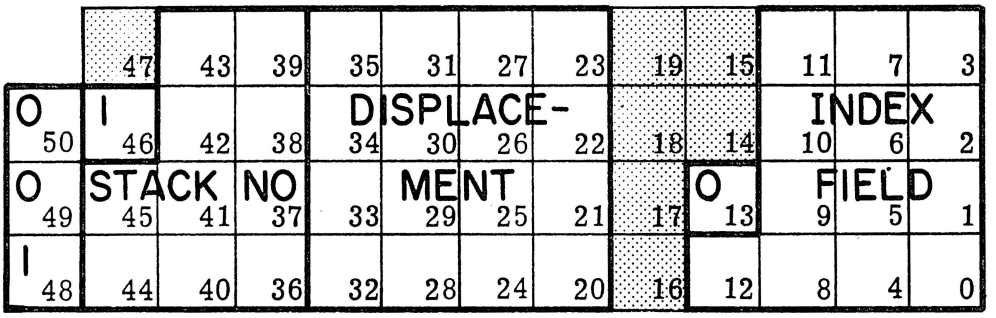
PROGRAM LEVEL 0-31



NOTE: THE BIT ORDER OF THE LL FIELD IS INVERTED.

40983

STUFFED INDIRECT REFERENCE WORD



Field	Bits	Description
Tag	50:3	Tag field. Value equals one.
	47:1	Not used.
	46:1	Environment bit. Must be a one (0=IRW).
STACK NO.	45:10	The number of the stack containing the referenced word.
DISPLACEMENT	35:16	This number, added to the stack base address, addresses an MSCW.
	19:6	Not used.
	13:1	Must be 0.
INDEX FIELD	12:13	This number, added to the address of the MSCW, addresses the referenced word.

40984

DOUBLE PRECISION OPERAND

DOUBLE PRECISION OPERAND (OCTAL REPRESENTATION)

FIRST WORD

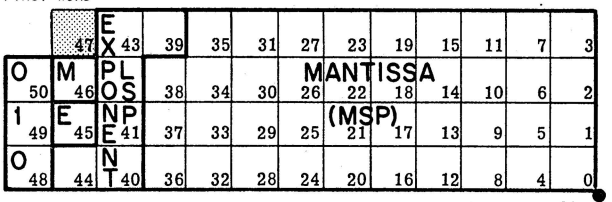


SECOND WORD

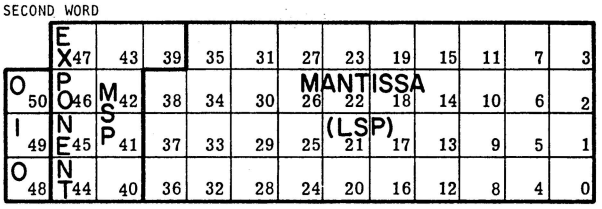


DOUBLE PRECISION OPERAND (HEXADECIMAL REPRESENTATION)

FIRST WORD



SECOND WORD



First Word

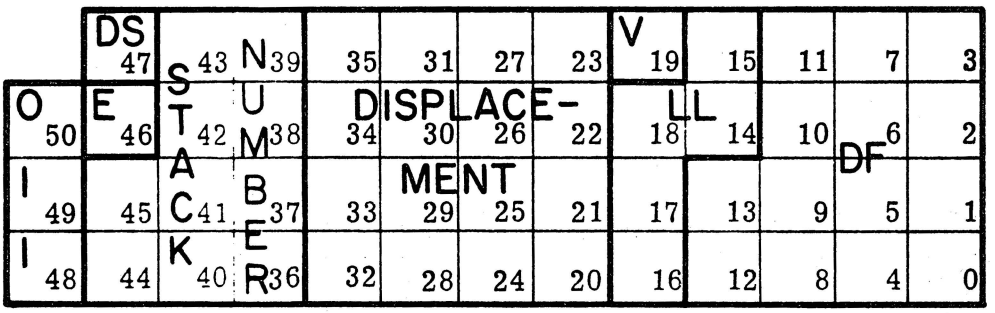
Field	Bits	Description
TAG	50:3	010
	47:1	Not used
M	46:1	1 = negative, 0 = positive.
E	45:1	Sign of exponent.
		1 = negative, 0 = positive.
EXPONENT LSP	44:6	Least significant portion of exponent.
MANTISSA MSP	38:39	Most significant portion of mantissa.

Second Word

Field	Bits	Description
TAG	50:13	010
EXPONENT MSP	47:9	Most significant portion of exponent.
MANTISSA LSP	38:39	Least significant portion of mantissa.

40962

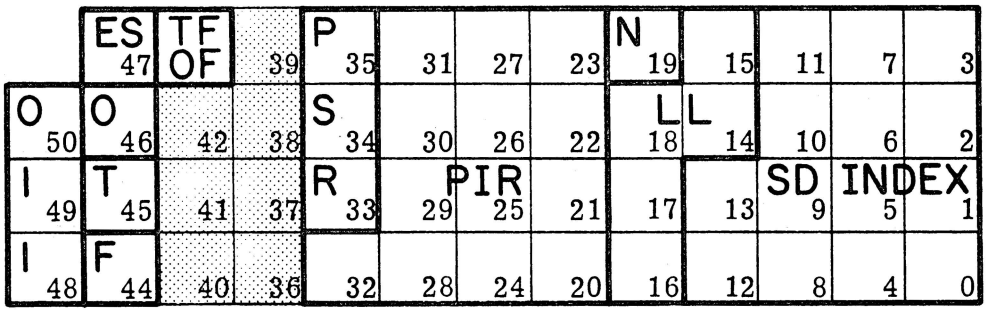
MARK STACK CONTROL WORD



Field	Bits	Description
Tag	50:3	Tag field. Value equals three.
DS	47:1	Different-stack bit. A 0 indicates that the stack-number field refers to the current stack. A 1 indicates that the stack-number field refers to a different stack.
E	46:1	Environment bit. A 0 indicates an inactive MSCW, generated directly by the Mark Stack operator. The procedure entry has not been performed. A 1 denotes an active MSCW generated upon entry into a procedure, at which time the environment fields (stack number, displacement, value, and LL fields) are stored into the MSCW.
STACK NUMBER	45:10	Stack-number field. Contains the number of the stack from which the PCW was obtained at procedure-entry.
DISPLACEMENT	35:16	Displacement field. When added to the stack base address, locates the MSCW of the prior lexicographic level.
V	19:1	Value bit. A 0 indicates that the MSCW was generated during any operation that will be restarted from the beginning. A 1 indicates that the operator must continue after the Exit or Return which refers to this MSCW (e.g., an accidental entry by a Value Call).
LL	18:5	LL field. Denotes the lexicographical level at which the program will run when the procedure is entered.
DF	13:14	Denotes the stack history. This field is used to locate, in the stack, the preceding MSCW (i.e., the previous "F" register setting).

40985

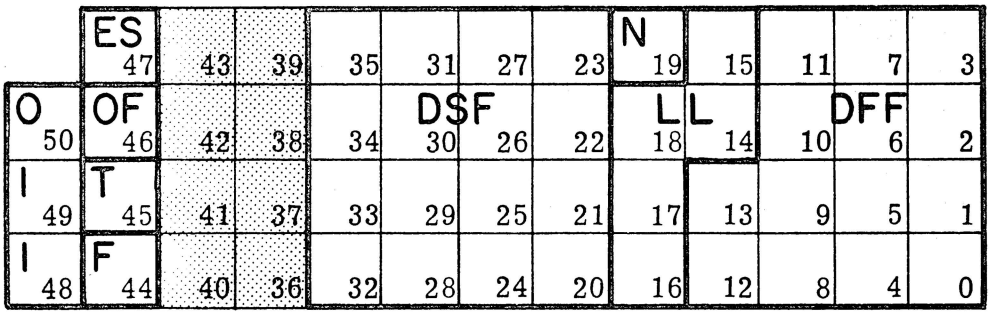
RETURN CONTROL WORD



Field	Bits	Description
Tag	50:3	Tag field. Value of three.
ES	47:1	External Sign flip-flop.
O	46:1	Overflow flip-flop.
T	45:1	True/False flip-flop.
F	44:1	Float flip-flop.
TFOF	43:1	True/False Flip-flop occupied flip-flop.
	42:7	Not used.
PSR	35:3	Program syllable of the operator to be executed after return from the subroutine.
PIR	32:13	PIR setting of the operator to be executed next in the calling routine.
N	19:1	Normal state (0) or control state (1) procedure.
LL	18:5	Level of the calling procedure when the RCW was generated (at procedure entry).
SD INDEX	13:14	Segment descriptor index. Bits 12 through 0 specify the value to be added to the address located by either D-register 0 or 1. When bit 13 = 0, D-register is selected; when bit 13 = 1, D register 1 is selected.

40986

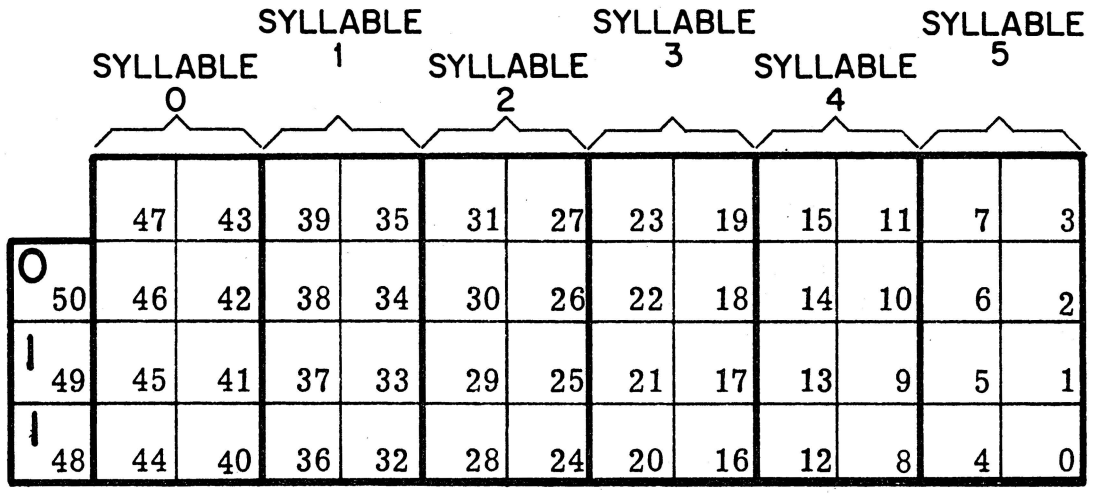
TOP OF STACK CONTROL WORD



Field	Bits	Description
Tag	50:3	Tag field. Value equals three.
ES	47:1	External sign flip-flop.
OF	46:1	Overflow flip-flop.
T	45:1	True/False flip-flop.
F	44:1	Float flip-flop.
	43:8	Not used.
DSF	35:16	Delta S-register field. The value of S-register displacement above BOSR.
N	19:1	Normal-control state flip-flop. 0 = normal; 1 = control state.
LL	18:5	Lexicographic level.
DFF	13:14	Delta F-register field. The value of F-register displacement below the S-register.

40987

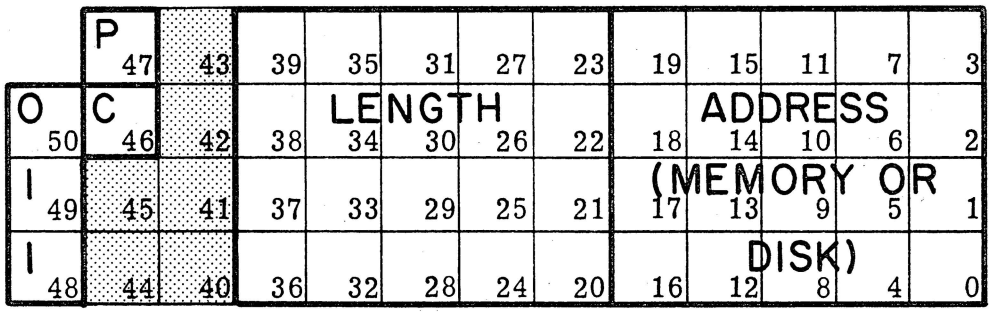
PROGRAM WORD



Field	Bits	Description
Tag	50:3	Tag field. Value of three indicates that this word is non-modifiable (except by Overwrite operators).
	47:8	Syllable 0
	39:8	Syllable 1
	31:8	Syllable 2
	23:8	Syllable 3
	15:8	Syllable 4
	7:8	Syllable 5

40968

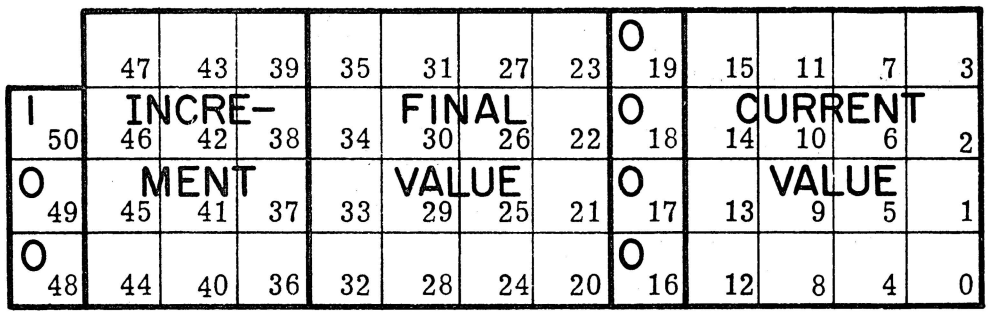
SEGMENT DESCRIPTOR



Field	Bits	Description
Tag	50:3	Tag field. Value equals three.
P	47:1	Presence bit. A 0 indicates that the segment is absent from main memory.
C	46:1	Copy bit. A 0 indicates that this is the original segment descriptor. A 1 indicates that this is a copy of the original segment descriptor.
	45:4	Not used. Unused bits may be either 0 or 1.
LENGTH	39:20	The length of the program segment in words.
ADDRESS (MEMORY OR DISK)	19:20	This field contains either the main memory address or the disk file address. If the presence bit (bit 47 equals 1, the field contains the main memory address of the program segment. If both the presence bit and the copy bit (bit 46) equal 0, the field contains the disk address of the non-present program segment. If the presence bit equals 0 and the copy bit equals 1, the field contains the absolute memory address of the original program segment descriptor.

40981

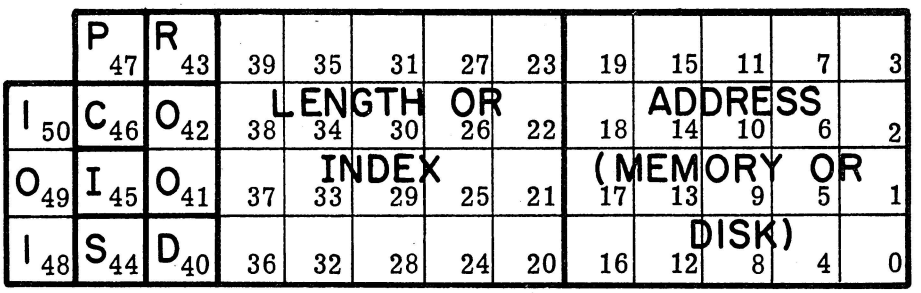
STEP INDEX WORD



Field	Bits	Description
Tag	50:3	Tag field. Value equals four.
INCREMENT	47:12	Increment: value to be added to current value field.
FINAL VALUE	35:16	Final value: value used to terminate the iteration loop.
	19:4	Must be 0 for SIW.
CURRENT VALUE	15:16	Current value or count. The branch is made if this field is greater than the final value field.

40988

DATA DESCRIPTOR

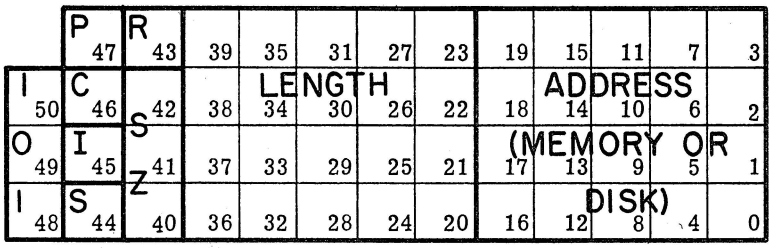


Field	Bits	Description
Tag	50:3	Tag field. Value of five.
P	47:1	Presence bit. Indicates the presence or absence of data in main memory. A 0 causes a presence bit interrupt whenever the descriptor is used by a processor to obtain non-present data. A 1 indicates that the data described is in main memory.
C	46:1	Copy bit. A 0 indicates that this is the original descriptor for the particular data area. A 1 indicates that this descriptor is a copy of the original descriptor.
I	45:1	Indexed bit. A 0 indicates that an indexing operation is required before the descriptor may be used to obtain data. A 1 indicates that indexing has already taken place and the index value is stored in bit positions 39:20 (Length or Index).
S	44:1	Segmented bit. A 0 indicates that the data is not segmented. A 1 indicates that the data is divided into segments.
R	43:1	Read-only bit. A 0 indicates that the data may be referenced for reading or writing. A 1 indicates that the area cannot be used for data storage.
	42:2	Size field, must be 0 to indicate a data descriptor.
D	40:1	Double-precision bit. A 0 indicates single-precision operands, a 1 indicates double-precision operands.
LENGTH OR INDEX	39:20	This field contains either the length (in operands) of the memory area (if bit 45 = 0) or an index value (if bit 45 = 1). If bit 45 equals 0, the descriptor has not been indexed. This field is used for size checking during the indexing operation. If bit 45 equals 1, the descriptor has been indexed. For a double-precision operation, the index is doubled after index size checking, and the result is stored in the index field.
ADDRESS (MEMORY OR DISK)	19:20	This field contains either a main memory or disk address. If the presence bit (bit 47) equals 1, this field contains the memory address of data. If the presence bit equals 0 and the copy bit (bit 46) equals 0, this field contains the disk address of the data. If the presence bit equals 0 and the copy bit equals 1, this field contains the memory address of the original descriptor.

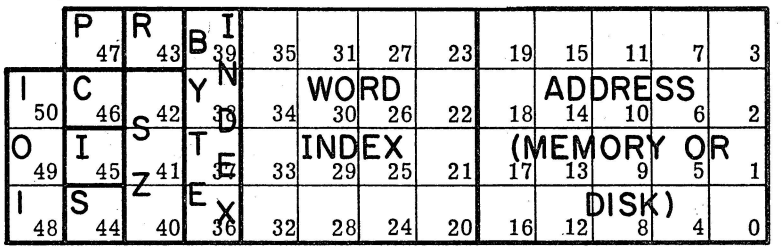
40979

STRING DESCRIPTOR

STRING DESCRIPTOR (NON-INDEXED)



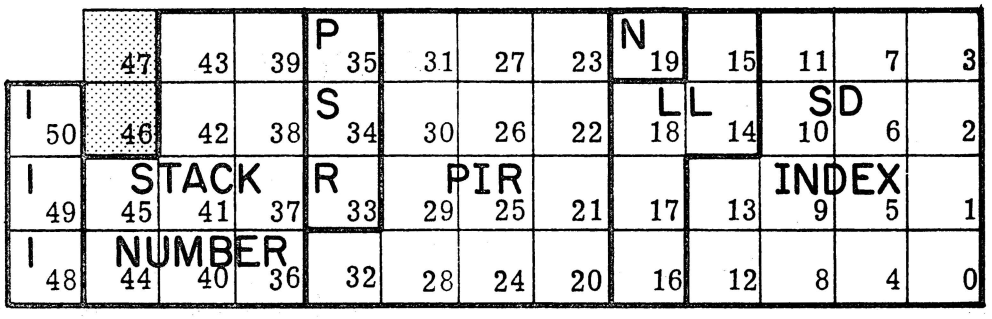
STRING DESCRIPTOR (INDEXED)



Field	Bits	Description
Tag	50:3	Tag field. Value of five.
P	47:1	Presence bit. A 0 causes a presence bit interrupt if the descriptor is used to access data. A 1 indicates the data is present in main memory.
C	46:1	Copy bit. A 0 indicates that this is the original descriptor for the particular data area. A 1 indicates that this descriptor is a copy of the original descriptor.
I	45:1	Indexed bit. A 0 indicates indexing is required. A 1 indicates that indexing has taken place and the word and character index are in the WORD INDEX and BYTE INDEX fields.
S	44:1	Segmented bit. A 0 indicates that the data area is not segmented. A 1 indicates that the data is segmented.
R	43:1	Read only bit. A 0 indicates that the data may be referenced for reading or writing. A 1 indicates that the data can be read only.
SZ	42:3	Size field. 100 indicates character size of 8-bit bytes, 101 indicates 7-bit ASCII characters, 011 indicates 6-bit characters, and 010 indicates 4-bit digits.
LENGTH	39:20	Bits 39:20, contain either the length of the memory area (bit 45=0) or an index value (bit 45=1). When bit 45 equals 0, this field contains the length of the area in digits, characters or bytes.
BYTE INDEX	39:4	Byte index (Bit 45=1).
WORD INDEX	35:16	Word Index (Bit 45=1).
ADDRESS (MEMORY OR DISK)	19:20	This field contains either a main memory or a disk address. If the presence bit (bit 47) is 1, the field contains a memory address of the data. If both the presence bit and the copy bit (bit 46) are equal to 0, the field contains the disk address of the non-present data. If the presence bit is 0 and the copy bit is 1, the field contains the memory address of the original descriptor.

40980

PROGRAM CONTROL WORD



Field	Bits	Description
Tag	50:3	Tag field. Value equals seven.
	47:2	Not used.
STACK NUMBER	45:10	The number of the stack which contains the PCW.
PSR	35:3	The program syllable (0-5) within the word located by PIR.
PIR	32:13	Index to the Program Base Register. Locates a word within the code segment.
N	19:1	Normal state (0) or control state (1).
LL	18:5	The level of the procedure being entered.
SD INDEX	13:14	The segment descriptor index. Bits 12 through 0 specify the value to be added to the address located by either D-register 0 or 1. When bit 13 equals 0, D-register 0 is selected; when bit 13 equals 1, D-register 1 is selected. Locates a segment descriptor.

40982

APPENDIX H
PROCESSOR OPERATORS BY MNEMONICS

MNEMONIC	MODE ID & HEX CODE	OPERATOR NAME	PAGE
ADD	(P)80	ADD	3-105
BRFL	(P)A0	BRANCH ON FALSE	3-108
BRST	(P)9E	BIT RESET	3-107
BRTR	(P)A1	BRANCH ON TRUE	3-108
BRUN	(P)A2	BRANCH UNCONDITIONAL	3-108
BSET	(P)96	BIT SET	3-107
CBON	(V)BB	COUNT BINARY ONES	3-107
CEQD	(P)F4	COMPARE CHARACTERS EQUAL, DESTRUCTIVE	3-110
CEQU	(P)FC	COMPARE CHARACTERS EQUAL, UPDATE	3-110
CGED	(P)F1	COMPARE CHARACTERS GREATER OR EQUAL, DESTRUCTIVE	3-110
CGEU	(P)F9	COMPARE CHARACTERS GREATER OR EQUAL, UPDATE	3-110
CGTD	(P)F2	COMPARE CHARACTERS GREATER, DESTRUCTIVE	3-110
CGTU	(P)FA	COMPARE CHARACTERS GREATER, UPDATE	3-110
CHSN	(P)8E	CHANGE SIGN BIT	3-107
CLED	(P)F3	COMPARE CHARACTERS LESS OR EQUAL, DESTRUCTIVE	3-111
CLEU	(P)FB	COMPARE CHARACTERS LESS OR EQUAL, UPDATE	3-111
CLSD	(P)F0	COMPARE CHARACTERS LESS, DESTRUCTIVE	3-111
CLSU	(P)F8	COMPARE CHARACTERS LESS, UPDATE	3-111
CNED	(P)F5	COMPARE CHARACTERS NOT EQUAL, DESTRUCTIVE	3-111
CNEU	(P)FD	COMPARE CHARACTERS NOT EQUAL, UPDATE	3-111
DBFL	(P)A8	DYNAMIC BRANCH FALSE	3-109
DBRS	(P)9F	DYNAMIC BIT RESET	3-107
DBST	(P)97	DYNAMIC BIT SET	3-107
DBTR	(P)A9	DYNAMIC BRANCH TRUE	3-108
DBUN	(P)AA	DYNAMIC BRANCH UNCONDITIONAL	3-108
DEXI	(V)47	DISABLE EXTERNAL INTERRUPTS	3-152
DFTR	(P)99	DYNAMIC FIELD TRANSFER	3-139
DINS	(P)9D	DYNAMIC FIELD INSERT	3-142
DISO	(P)9B	DYNAMIC FIELD ISOLATE	3-142
DIVD	(P)83	DIVIDE	3-106
DLA	(Z)F0	DOUBLE LOAD A	3-168
DLAI	(Z)F1	DOUBLE LOAD A INCREMENT	3-169
DLB	(Z)F2	DOUBLE LOAD B	3-168
DLBI	(Z)F3	DOUBLE LOAD B INCREMENT	3-169
DLC	(Z)F4	DOUBLE LOAD C	3-168
DLCI	(Z)F5	DOUBLE LOAD C INCREMENT	3-169

PROCESSOR OPERATORS, BY MNEMONICS

MNEMONIC	MODE ID & HEX CODE	OPERATOR NAME	PAGE
DLET	(P)B5	DELETE TOP OF STACK	3-125
DSA	(Z)F8	DOUBLE STORE A	3-169
DSAI	(Z)F9	DOUBLE STORE A INCREMENT	3-169
DSB	(Z)FA	DOUBLE STORE B	3-169
DSBI	(Z)FB	DOUBLE STORE B INCREMENT	3-169
DSC	(Z)FC	DOUBLE STORE C	3-169
DSCI	(Z)FD	DOUBLE STORE C INCREMENT	3-169
DSLF	(P)C1	DYNAMIC SCALE LEFT	3-123
DSRF	(P)C7	DYNAMIC SCALE RIGHT FINAL	3-124
DSRR	(P)C9	DYNAMIC SCALE RIGHT ROUNDED	3-124
DSRS	(P)C5	DYNAMIC SCALE RIGHT SAVE	3-124
DSRT	(P)C3	DYNAMIC SCALE RIGHT TRUNCATE	3-124
DUPL	(P)B7	DUPLICATE TOP OF STACK	3-125
EEXI	(V)46	ENABLE EXTERNAL INTERRUPTS	3-151
ENDE	(E)DE	END EDIT	3-164
ENDF	(E)D5	END FLOAT	3-163
ENTR	(P)AB	ENTER	3-136
EQUL	(P)8C	EQUAL	3-122
EVAL	(P)AC	EVALUATE DESCRIPTOR	3-136
EXCH	(P)B6	EXCHANGE	3-125
EXIT	(P)A3	EXIT	3-136
EXPU	(P)DD	EXECUTE SINGLE MICRO, SINGLE POINTER UPDATE	3-112
EXSD	(P)D2	EXECUTE SINGLE MICRO, DESTRUCTIVE	3-112
EXSU	(P)DA	EXECUTE SINGLE MICRO, UPDATE	3-112
FLTR	(P)98	FIELD TRANSFER	3-139
FMFR	(V)AC	FETCH MEMORY FAIL REGISTER	3-158
FTCH	(Z)00 → 3F	VECTOR FETCH	3-170
GREQ	(P)89	GREATER THAN OR EQUAL	3-122
GRTR	(P)8A	GREATER THAN	3-122
HALT	(P)DF	CONDITIONAL HALT	3-143
HALT	(V)DF	CONDITIONAL HALT	3-159
HALT	(E)DF	CONDITIONAL HALT	3-164
ICVD	(P)CA	INPUT CONVERT, DESTRUCTIVE	3-119
ICVU	(P)CB	INPUT CONVERT, UPDATE	3-119
IDIV	(P)84	INTEGER DIVIDE	3-106
IDLE	(V)44	IDLE UNTIL INTERRUPT	3-152
IGPR	(V)48	IGNORE PARITY	3-158
IMKS	(P)CF	INSERT MARK STACK	3-133
INCN	(V)8F	INTERRUPT CHANNEL N	3-159

PROCESSOR OPERATORS, BY MNEMONICS

MNEMONIC	MODE ID & HEX CODE	OPERATOR NAME	PAGE
INDX	(P)A6	INDEX	3-117
INOP	(E)D8	INSERT OVERPUNCH	3-161
INSC	(E)DD	INSERT CONDITIONAL	3-161
INSG	(E)D9	INSERT DISPLAY SIGN	3-161
INSR	(P)9C	FIELD INSERT	3-142
INSU	(E)DC	INSERT UNCONDITIONAL	3-161
ISOL	(P)9A	FIELD ISOLATE	3-139
JOIN	(V)42	SET TWO SINGLES TO DOUBLE	3-142
LAND	(P)90	LOGICAL AND	3-120
LDA	(Z)E0	LOAD A	3-167
LDAI	(Z)E1	LOAD A INCREMENT	3-168
LDB	(Z)E2	LOAD B	3-167
LDBI	(Z)E3	LOAD B INCREMENT	3-168
LDC	(Z)E4	LOAD C	3-167
LDCI	(Z)E5	LOAD C INCREMENT	3-168
LEQV	(P)93	LOGICAL EQUIVALENCE	3-121
LESS	(P)88	LESS THAN	3-123
LLLU	(V)BD	LINKED LIST LOCKUP	3-155
LNOT	(P)92	LOGICAL NEGATE	3-121
LOAD	(P)BD	LOAD	3-118
LODT	(V)BC	LOAD TRANSPARENT	3-118
LOG2	(V)8B	LEADING ONE TEST	3-107
LOR	(P)91	LOGICAL OR	3-121
LSEQ	(P)8B	LESS THAN OR EQUAL	3-122
LT16	(P)B3	LIT CALL 16 BITS	3-120
LT48	(P)BE	LIT CALL 48 BITS	3-120
LT8	(P)B2	LIT CALL 8 BITS	3-120
MCHR	(E)D7	MOVE CHARACTERS	3-162
MFLT	(E)D1	MOVE WITH FLOAT	3-162
MINS	(E)D0	MOVE WITH INSERT	3-162
MKST	(P)AE	MARK STACK	3-132
MPCW	(P)BF	MAKE PROGRAM CONTROL WORD	3-120
MULT	(P)82	MULTIPLY	3-106
MULX	(P)8F	EXTENDED MULTIPLY	3-106
MVNU	(E)D6	MOVE NUMERIC UNCONDITIONAL	3-163
MVST	(V)AF	MOVE TO STACK	3-156

PROCESSOR OPERATORS, BY MNEMONICS

MNEMONIC	MODE ID & HEX CODE	OPERATOR NAME	PAGE
NAMC	(P)40 → 7F	NAME CALL	3-133
NEQL	(P)8D	NOT EQUAL	3-123
NOOP	(P)FE	NO OPERATION	3-143
NOOP	(V)FE	NO OPERATION	3-159
NOOP	(E)FE	NO OPERATION	3-164
NOOP	(Z)FE	NO OPERATION	3-170
NTGD	(V)87	INTEGERIZE, ROUNDED, DOUBLE PRECISION	3-107
NTGR	(P)87	INTEGERIZE, ROUNDED	3-106
NTIA	(P)86	INTEGERIZE, TRUNCATED	3-106
NVLD	(P)FF	INVALID OPERATOR	3-143
NVLD	(V)FF	INVALID OPERATOR	3-159
NVLD	(E)FF	INVALID OPERATOR	3-164
NVLD	(Z)FF	INVALID OPERATOR	3-170
NXLN	(P)A5	INDEX AND LOAD NAME	3-118
NXLV	(P)AD	INDEX AND LOAD VALUE	3-118
OCRX	(V)85	OCCURS INDEX	3-157
ONE	(P)B1	LIT CALL ONE	3-120
OVRD	(P)BA	OVERWRITE DESTRUCTIVE	3-126
OVRN	(P)BB	OVERWRITE NON-DESTRUCTIVE	3-126
PACD	(P)D1	PACK DESTRUCTIVE	3-121
PACU	(P)D9	PACK UPDATE	3-122
PAUS	(V)84	PAUSE UNTIL INTERRUPT	3-158
PUSH	(P)B4	PUSH DOWN STACK REGISTERS	3-125
RDIV	(P)85	REMAINDER DIVIDE	3-106
RDLK	(V)BA	READ WITH LOCK	3-126
RETN	(P)A7	RETURN	3-139
ROFF	(P)D7	READ AND CLEAR OVERFLOW FLIP-FLOP	3-143
RPRR	(V)B8	READ PROCESSOR REGISTER	3-152
RSDN	(V)B7	ROTATE STACK DOWN	3-125
RSTF	(E)D4	RESET FLOAT	3-163
RSUP	(V)B6	ROTATE STACK UP	3-125
RTAG	(V)B5	READ TAG FIELD	3-151
RTFF	(P)DE	READ TRUE/FALSE FLIP-FLOP	3-143
SAME	(P)94	LOGICAL EQUAL	3-123
SCLF	(P)C0	SCALE LEFT	3-123
SCNI	(V)4A	SCAN IN (TOD ONLY)	3-148
SCRF	(P)C6	SCALE RIGHT FINAL	3-124
SCRR	(P)C8	SCALE RIGHT ROUNDED	3-124
SCRS	(P)C4	SCALE RIGHT SAVE	3-124
SCRT	(P)C2	SCALE RIGHT TRUNCATE	3-124
SEQD	(V)F4	SCAN WHILE EQUAL, DESTRUCTIVE	3-149
SEQU	(V)FC	SCAN WHILE EQUAL, UPDATE	3-149

PROCESSOR OPERATORS, BY MNEMONICS

MNEMONIC	MODE ID & HEX CODE	OPERATOR NAME	PAGE
SFDC	(E)DA	SKIP FORWARD DESTINATION CHARACTERS	3-163
SFSC	(E)D2	SKIP FORWARD SOURCE CHARACTERS	3-163
SGED	(V)F1	SCAN WHILE GREATER OR EQUAL, DESTRUCTIVE	3-148
SGEU	(V)F9	SCAN WHILE GREATER OR EQUAL, UPDATE	3-149
SGTD	(V)F2	SCAN WHILE GREATER, DESTRUCTIVE	3-148
SGTU	(V)FA	SCAN WHILE GREATER, UPDATE	3-148
SINH	(V)A8	SET MEMORY INHIBITS	3-158
SINT	(V)45 C	SET INTERVAL TIMER	3-151
SISO	(P)D5	STRING ISOLATE	3-128
SLED	(V)F3	SCAN WHILE LESS OR EQUAL, DESTRUCTIVE	3-150
SLEU	(V)FB	SCAN WHILE LESS OR EQUAL, UPDATE	3-150
SLMT	(V)AA	SET MEMORY LIMITS	3-158
SLSD	(V)F0	SCAN WHILE LESS, DESTRUCTIVE	3-150
SLSU	(V)F8	SCAN WHILE LESS, UPDATE	3-150
SNED	(V)F5	SCAN WHILE NOT EQUAL, DESTRUCTIVE	3-150
SNEU	(V)FD	SCAN WHILE NOT EQUAL, UPDATE	3-150
SNGL	(P)CD	SET TO SINGLE PRECISION, ROUNDED	3-142
SNGT	(P)CC	SET TO SINGLE PRECISION, TRUNCATED	3-142
SPLT	(V)43	SET DOUBLE TO TWO SINGLES	3-142
SPRR	(V)B9	SET PROCESSOR REGISTER	3-152
SRCH	(V)BE	MASKED SEARCH FOR EQUAL	3-156
SRDC	(E)DB	SKIP REVERSE DESTINATION CHARACTERS	3-163
SRSC	(E)D3	SKIP REVERSE SOURCE CHARACTER	3-163
STA	(Z)E8	STORE A	3-168
STAG	(V)B4	SET TAG FIELD	3-151
STAI	(Z)E9	STORE A INCREMENT	3-168
STB	(Z)EA	STORE B	3-168
STBI	(Z)EB	STORE B INCREMENT	3-168
STBR	(P)A4	STEP AND BRANCH	3-109
STC	(Z)EC	STORE C	3-168
STCI	(Z)ED	STORE C INCREMENT	3-168
STFF	(P)AF	STUFF ENVIRONMENT	3-143
STOD	(P)B8	STORE DESTRUCTIVE	3-125
STON	(P)B9	STORE NON-DESTRUCTIVE	3-126
STOP	(V)BF	STOP	3-159
STOR	(Z)40 → 7F	VECTOR STORE	3-170
SUBT	(P)81	SUBTRACT	3-106

PROCESSOR OPERATORS, BY MNEMONICS

MNEMONIC	MODE ID & HEX CODE	OPERATOR NAME	PAGE
SWFD	(V)D4	SCAN WHILE FALSE, DESTRUCTIVE	3-151
SWFU	(V)DC	SCAN WHILE FALSE, UPDATE	3-151
SWTD	(V)D5	SCAN WHILE TRUE, DESTRUCTIVE	3-150
SWTU	(V)DD	SCAN WHILE TRUE, UPDATE	3-151
SXSN	(P)D6	SET EXTERNAL SIGN	3-143
TEED	(P)D0	TABLE ENTER EDIT, DESTRUCTIVE	3-111
TEEU	(P)D8	TABLE ENTER EDIT, UPDATE	3-112
TEQD	(P)E4	TRANSFER WHILE EQUAL, DESTRUCTIVE	3-130
TEQU	(P)EC	TRANSFER WHILE EQUAL, UPDATE	3-130
TGED	(P)E1	TRANSFER WHILE GREATER OR EQUAL, DESTRUCTIVE	3-130
TGEU	(P)E9	TRANSFER WHILE GREATER OR EQUAL, UPDATE	3-130
TGTD	(P)E2	TRANSFER WHILE GREATER, DESTRUCTIVE	3-129
TGTU	(P)EA	TRANSFER WHILE GREATER, UPDATE	3-130
TLED	(P)E3	TRANSFER WHILE LESS OR EQUAL, DESTRUCTIVE	3-130
TLEU	(P)EB	TRANSFER WHILE LESS OR EQUAL, UPDATE	3-130
TLSD	(P)E0	TRANSFER WHILE LESS, DESTRUCTIVE	3-131
TLSU	(P)E8	TRANSFER WHILE LESS, UPDATE	3-131
TNED	(P)E5	TRANSFER WHILE NOT EQUAL, DESTRUCTIVE	3-131
TNEU	(P)ED	TRANSFER WHILE NOT EQUAL, UPDATE	3-131
TRNS	(V)D7	TRANSLATE	3-157
TUND	(P)E6	TRANSFER UNCONDITIONAL, DESTRUCTIVE	3-132
TUNU	(P)EE	TRANSFER UNCONDITIONAL, UPDATE	3-132
TWFD	(V)D2	TRANSFER WHILE FALSE, DESTRUCTIVE	3-132
TWFU	(V)DA	TRANSFER WHILE FALSE, UPDATE	3-132
TWOD	(P)D41	TRANSFER WORDS OVERWRITE, DESTRUCTIVE	3-129
TWOU	(P)DC	TRANSFER WORDS OVERWRITE, UPDATE	3-129
TWSD	(P)D3	TRANSFER WORDS, DESTRUCTIVE	3-128
TWSU	(P)DB	TRANSFER WORDS, UPDATE	3-129
TWTD	(V)D3	TRANSFER WHILE TRUE, DESTRUCTIVE	3-131
TWTU	(V)DB	TRANSFER WHILE TRUE, UPDATE	3-132
UABD	(V)D1	UNPACK ABSOLUTE, DESTRUCTIVE	3-154
UABU	(V)D9	UNPACK ABSOLUTE, UPDATE	3-154
USND	(V)D0	UNPACK SIGNED, DESTRUCTIVE	3-155

PROCESSOR OPERATORS, BY MNEMONICS

MNEMONIC	MODE ID & HEX CODE	OPERATOR NAME	PAGE
USNU	(V)D8	UNPACK SIGNED, UPDATE	3-155
VALC	(P)00 → 3F	VALUE CALL	3-133
VARI	(P)95	ESCAPE TO 16-BIT INSTRUCTION	3-143
VEBR		VECTOR BRANCH	3-167
VMOM	(Z)EF	VECTOR MODE, MULTIPLE WORD	3-117
VMOS	(Z)E7	VECTOR MODE, SINGLE WORD	3-117
VXIT	(Z)E6	VECTOR EXIT	3-167
WHOI	(V)4E	READ PROCESSOR IDENTIFICATION	3-151
XTND	(P)CE	SET TO DOUBLE PRECISION	3-142
ZERO	(P)B0	LIT CALL ZERO	3-119

APPENDIX I
PROCESSOR OPERATORS, BY NAME

OPERATOR NAME	MNEMONIC	MODE ID & HEX CODE	PAGE
ADD	ADD	(P)80	3-105
BIT RESET	BRST	(P)9E	3-107
BIT SET	BSET	(P)96	3-107
BRANCH ON FALSE	BRFL	(P)A0	3-108
BRANCH ON TRUE	BRTR	(P)A1	3-108
BRANCH UNCONDITIONAL	BRUN	(P)A2	3-108
CHANGE SIGN BIT	CHSN	(P)8E	3-107
COMPARE CHARACTERS EQUAL, DESTRUCTIVE	CEQD	(P)F4	3-110
COMPARE CHARACTERS EQUAL, UPDATE	CEQU	(P)FC	3-110
COMPARE CHARACTERS GREATER OR EQUAL, DESTRUCTIVE	CGED	(P)F1	3-110
COMPARE CHARACTERS GREATER OR EQUAL, UPDATE	CGEU	(P)F9	3-110
COMPARE CHARACTERS GREATER, DESTRUCTIVE	CGTD	(P)F2	3-110
COMPARE CHARACTERS GREATER, UPDATE	CGTU	(P)FA	3-110
COMPARE CHARACTERS LESS OR EQUAL, DESTRUCTIVE	CLED	(P)F3	3-111
COMPARE CHARACTERS LESS OR EQUAL, UPDATE	CLEU	(P)FB	3-111
COMPARE CHARACTERS LESS, DESTRUCTIVE	CLSD	(P)F0	3-111
COMPARE CHARACTERS LESS, UPDATE	CLSU	(P)F8	3-111
COMPARE CHARACTERS NOT EQUAL, DESTRUCTIVE	CNED	(P)F5	3-111
COMPARE CHARACTERS NOT EQUAL, UPDATE	CNEU	(P)FD	3-111
CONDITIONAL HALT	HALT	(P)DF	3-143
CONDITIONAL HALT	HALT	(V)DF	3-159
CONDITIONAL HALT	HALT	(E)DF	3-164
COUNT BINARY ONES	CBON	(V)BB	3-107
DELETE TOP OF STACK	DLET	(P)B5	3-125
DISABLE EXTERNAL INTERRUPTS	DEXI	(V)47	3-152
DIVIDE	DIVD	(P)83	3-108
DOUBLE LOAD A	DLA	(Z)F0	3-168
DOUBLE LOAD A INCREMENT	DLAI	(Z)F1	3-169
DOUBLE LOAD B	DLB	(Z)F2	3-168
DOUBLE LOAD B INCREMENT	DLBI	(Z)F3	3-169
DOUBLE LOAD C	DLC	(Z)F4	3-168
DOUBLE LOAD C INCREMENT	DLCI	(Z)F5	3-169
DOUBLE STORE A	DSA	(Z)F8	3-169
DOUBLE STORE A INCREMENT	DSAI	(Z)F9	3-169
DOUBLE STORE B	DSB	(Z)FA	3-169
DOUBLE STORE B INCREMENT	DSBI	(Z)FB	3-169
DOUBLE STORE C	DSC	(Z)FC	3-169
DOUBLE STORE C INCREMENT	DSCI	(Z)FD	3-169
DUPLICATE TOP OF STACK	DUPL	(P)B7	3-125

APPENDIX I

PROCESSOR OPERATORS, BY NAME

OPERATOR NAME	MNEMONIC	MODE ID & HEX CODE	PAGE
DYNAMIC BIT RESET	DBRS	(P)9F	3-107
DYNAMIC BIT SET	DBST	(P)97	3-107
DYNAMIC BRANCH FALSE	DBFL	(P)A8	3-109
DYNAMIC BRANCH TRUE	DBTR	(P)A9	3-108
DYNAMIC BRANCH UNCONDITIONAL	DBUN	(P)AA	3-108
DYNAMIC FIELD INSERT	DINS	(P)9D	3-142
DYNAMIC FIELD ISOLATE	DISO	(P)9B	3-142
DYNAMIC FIELD TRANSFER	DFTR	(P)99	3-139
DYNAMIC SCALE LEFT	DSLF	(P)C1	3-123
DYNAMIC SCALE RIGHT FINAL	DSRF	(P)C7	3-124
DYNAMIC SCALE RIGHT ROUND	DSRP	(P)C9	3-124
DYNAMIC SCALE RIGHT SAVE	DSRS	(P)C5	3-124
DYNAMIC SCALE RIGHT TRUNCATE	DSRT	(P)C3	3-124
ENABLE EXTERNAL INTERRUPTS	EEXI	(V)46	3-151
END EDIT	ENDE	(E)DE	3-164
END FLOAT	ENDF	(E)D5	3-163
ENTER	ENTR	(P)AB	3-136
EQUAL	EQUL	(P)8C	3-122
ESCAPE TO 16-BIT INSTRUCTION	VARI	(P)95	3-143
EVALUATE DESCRIPTOR	EVAL	(P)AC	3-136
EXCHANGE	EXCH	(P)B6	3-125
EXECUTE SINGLE MICRO, SINGLE POINTER UPDATE	EXPU	(P)DD	3-112
EXECUTE SINGLE MICRO, DESTRUCTIVE	EXSD	(P)D2	3-163
EXECUTE SINGLE MICRO, UPDATE	EXSU	(P)DA	3-163
EXIT	EXIT	(P)A3	3-136
EXTENDED MULTIPLY	MULX	(P)8F	3-106
FETCH MEMORY FAIL REGISTER	FMFR	(V)AC	3-158
FIELD INSERT	INSR	(P)9C	3-142
FIELD ISOLATE	ISOL	(P)9A	3-139
FIELD TRANSFER	FLTR	(P)98	3-139
GREATER THAN	GRTR	(P)8A	3-122
GREATER THAN OR EQUAL	GREQ	(P)89	3-122
IDLE UNTIL INTERRUPT	IDLE	(V)44	3-152
IGNORE PARITY	IGPR	(V)48	3-158
INDEX	INDX	(P)A6	3-117

PROCESSOR OPERATORS, BY NAME

OPERATOR NAME	MNEMONIC	MODE ID & HEX CODE	PAGE
INDEX AND LOAD NAME	NXLN	(P)A5	3-118
INDEX AND LOAD VALUE	NXLV	(P)AD	3-118
INPUT CONVERT, DESTRUCTIVE	ICVD	(P)CA	3-119
INPUT CONVERT, UPDATE	ICVU	(P)CB	3-119
INSERT CONDITIONAL	INSC	(E)DD	3-161
INSERT DISPLAY SIGN	INSG	(E)D9	3-161
INSERT MARK STACK	IMKS	(P)CF	3-133
INSERT OVERPUNCH	INOP	(E)D8	3-161
INSERT UNCONDITIONAL	INSU	(E)DC	3-161
INTEGER DIVIDE	IDIV	(P)84	3-106
INTEGRIZE, ROUNDED	NTGR	(P)87	3-106
INTEGERIZE, ROUNDED, DOUBLE PRECISION	NTGD	(V)87	3-107
INTEGERIZE, TRUNCATED	NTIA	(P)86	3-106
INTERRUPT CHANNEL N	INCN	(V)8F	3-159
INVALID OPERATOR	NVLD	(P)FF	3-143
INVALID OPERATOR	NVLD	(V)FF	3-159
INVALID OPERATOR	NVLD	(E)FF	3-164
INVALID OPERATOR	NVLD	(Z)FF	3-170
LEADING ONE TEST	LOG2	(V)8B	3-107
LESS THAN	LESS	(P)88	3-123
LESS THAN OR EQUAL	LSEQ	(P)8B	3-122
LINKED LIST LOOKUP	LLLU	(V)BD	3-155
LIT CALL ONE	ONE	(P)B1	3-120
LIT CALL ZERO	ZERO	(P)B0	3-119
LIT CALL 16 BITS	LT16	(P)B3	3-120
LIT CALL 48 BITS	LT48	(P)BE	3-120
LIT CALL 8 BITS	LT8	(P)B2	3-120
LOAD	LOAD	(P)BD	3-118
LOAD A	LDA	(Z)E0	3-167
LOAD A INCREMENT	LDAI	(Z)E1	3-168
LOAD B	LDB	(Z)E2	3-167
LOAD B INCREMENT	LDBI	(Z)E3	3-168
LOAD C	LDC	(Z)E4	3-167
LOAD C INCREMENT	LDCI	(Z)E5	3-168
LOAD TRANSPARENT	LODT	(V)BC	3-118
LOGICAL AND	LAND	(P)90	3-120
LOGICAL EQUAL	SAME	(P)94	3-123
LOGICAL EQUIVALENCE	LEQV	(P)93	3-121
LOGICAL NEGATE	LNOT	(P)92	3-121

PROCESSOR OPERATORS, BY NAME

OPERATOR NAME	MNEMONIC	MODE ID & HEX CODE	PAGE
LOGICAL OR	LOR	(P)91	3-120
MAKE PROGRAM CONTROL WORD	MPCW	(P)BF	3-120
MARK STACK	MKST	(P)AE	3-132
MASKED SEARCH FOR EQUAL	SRCH	(V)BE	3-156
MOVE CHARACTERS	MCHR	(E)D7	3-162
MOVE NUMERIC UNCONDITIONAL	MVHU	(E)D6	3-163
MOVE TO STACK	MVST	(V)AF	3-156
MOVE WITH FLOAT	MFLT	(E)D1	3-162
MOVE WITH INSERT	MINS	(E)D0	3-162
MULTIPLE-WORD VECTOR MODE	VMOM	(P)EF	3-117
MULTIPLY	MULT	(P)82	3-106
NAME CALL	NAMC	(P)40 → 7F	3-133
NO OPERATION	NOOP	(P)FE	3-143
NO OPERATION	NOOP	(V)FE	3-159
NO OPERATION	NOOP	(E)FE	3-164
NO OPERATION	NOOP	(Z)FE	3-170
NOT EQUAL	NEQL	(P)8D	3-123
OCCURS INDEX	OCRX	(V)85	3-157
OVERWRITE DESTRUCTIVE	OVRD	(P)BA	3-126
OVERWRITE NON-DESTRUCTIVE	OVRN	(P)BB	3-126
PACK DESTRUCTIVE	PACD	(P)D1	3-121
PACK UPDATE	PACU	(P)D9	3-122
PAUSE UNTIL INTERRUPT	PAUS	(V)84	3-158
PUSH DOWN STACK REGISTERS	PUSH	(P)B4	3-125
READ AND CLEAR OVERFLOW FLIP-FLOP	ROFF	(P)D7	3-143
READ PROCESSOR IDENTIFICATION	WHOI	(V)4E	3-151
READ PROCESSOR REGISTER	RPRR	(V)B8	3-152
READ TAG FIELD	RTAG	(V)B5	3-151
READ TRUE/FALSE FLIP-FLOP	RTFF	(P)DE	3-143
READ WITH LOCK	RDLK	(V)BA	3-126
REMAINDER DIVIDE	RDIV	(P)85	3-106
RESET FLOAT	RSIF	(E)D4	3-163
RETURN	RETN	(P)A7	3-139
ROTATE STACK DOWN	RSDN	(V)B7	3-125
ROTATE STACK UP	RSUP	(V)B6	3-125
SCALE LEFT	SCLF	(P)C0	3-123
SCALE RIGHT FINAL	SCRF	(P)C6	3-124
SCALE RIGHT ROUND	SCRR	(P)C8	3-124
SCALE RIGHT SAVE	SCRS	(P)C4	3-124
SCALE RIGHT TRUNCATE	SCRT	(P)C2	3-124

PROCESSOR OPERATORS BY NAME

OPERATOR NAME	MNEMONIC	MODE ID & HEX CODE	PAGE
SCAN IN	SCNI	(V)4A	3-148
SCAN WHILE EQUAL, DESTRUCTIVE	SEQD	(V)F4	3-149
SCAN WHILE EQUAL, UPDATE	SEQU	(V)FC	3-149
SCAN WHILE FALSE, DESTRUCTIVE	SWFD	(V)D4	3-151
SCAN WHILE FALSE, UPDATE	SWFU	(V)DC	3-151
SCAN WHILE GREATER OR EQUAL, DESTRUCTIVE	SGED	(V)F1	3-149
SCAN WHILE GREATER OR EQUAL, UPDATE	SGEU	(V)F9	3-141
SCAN WHILE GREATER, DESTRUCTIVE	SGTD	(V)F2	3-148
SCAN WHILE GREATER, UPDATE	SGTU	(V)FA	3-148
SCAN WHILE LESS OR EQUAL, DESTRUCTIVE	SLED	(V)F3	3-150
SCAN WHILE LESS OR EQUAL, UPDATE	SLEU	(V)FB	3-150
SCAN WHILE LESS, DESTRUCTIVE	SLSD	(V)F0	3-150
SCAN WHILE LESS, UPDATE	SLSU	(V)F8	3-150
SCAN WHILE NOT EQUAL, DESTRUCTIVE	SNED	(V)F5	3-150
SCAN WHILE NOT EQUAL, UPDATE	SNEU	(V)FD	3-150
SCAN WHILE TRUE, DESTRUCTIVE	SWTD	(V)D5	3-150
SCAN WHILE TRUE, UPDATE	SWTU	(V)DD	3-151
SET DOUBLE TO TWO SINGLES	SPLT	(V)43	3-142
SET EXTERNAL SIGN	SXSN	(P)D6	3-143
SET INTERVAL TIMER	SINT	(V)45	3-151
SET MEMORY INHIBITS	SINH	(V)A8	3-158
SET MEMORY LIMITS	SLMT	(V)AA	3-158
SET PROCESSOR REGISTER	SPRR	(V)B9	3-152
SET TAG FIELD	STAG	(V)B4	3-151
SET TO DOUBLE PRECISION	XTND	(P)CE	3-142
SET TO SINGLE PRECISION, ROUNDED	SNGL	(P)CD	3-142
SET TO SINGLE PRECISION, TRUNCATED	SNGT	(P)CC	3-142
SET TWO SINGLES TO DOUBLE	JOIN	(V)42	3-142
SINGLE-WORD VECTOR MODE	VMOS	(P)E7	3-117
SKIP FORWARD DESTINATION CHARACTERS	SFDC	(E)DA	3-163
SKIP FORWARD SOURCE CHARACTERS	SFSC	(E)D2	3-163
SKIP REVERSE DESTINATION CHARACTERS	SRDC	(E)DB	3-163
SKIP REVERSE SOURCE CHARACTERS	SRSC	(E)D3	3-163
STEP AND BRANCH	STBR	(P)A4	3-109
STOP	STOP	(V)BF	3-156
STORE DESTRUCTIVE	STOD	(P)B8	3-125
STORE NON-DESTRUCTIVE	STON	(P)B9	3-126
STRING ISOLATE	SIS0	(P)D5	3-128

PROCESSOR OPERATORS, BY NAME

OPERATOR NAME	MNEMONIC	MODE ID & HEX CODE	PAGE
STUFF ENVIRONMENT	STFF	(P)AF	3-143
SUBTRACT	SUBT	(P)81	3-106
TABLE ENTER EDIT, DESTRUCTIVE	TEED	(P)D0	3-111
TABLE ENTER EDIT, UPDATE	TEEU	(P)D8	3-111
TRANSFER UNCONDITIONAL, DESTRUCTIVE	TUND	(P)E6	3-132
TRANSFER UNCONDITIONAL, UPDATE	TUNU	(P)EE	3-132
TRANSFER WHILE EQUAL, DESTRUCTIVE	TEQD	(P)E4	3-130
TRANSFER WHILE EQUAL, UPDATE	TEQU	(P)EC	3-130
TRANSFER WHILE FALSE, DESTRUCTIVE	TWFD	(V)D2	3-132
TRANSFER WHILE FALSE, UPDATE	TWFU	(V)DA	3-132
TRANSFER WHILE GREATER OR EQUAL, DESTRUCTIVE	TGED	(P)E1	3-130
TRANSFER WHILE GREATER OR EQUAL, UPDATE	TGEU	(P)E9	3-130
TRANSFER WHILE GREATER, DESTRUCTIVE	TGTD	(P)E2	3-129
TRANSFER WHILE GREATER, UPDATE	TGTU	(P)EA	3-130
TRANSFER WHILE LESS OR EQUAL, DESTRUCTIVE	TLED	(P)E3	3-130
TRANSFER WHILE LESS OR EQUAL, UPDATE	TLEU	(P)EB	3-130
TRANSFER WHILE LESS, DESTRUCTIVE	TLSD	(P)E0	3-131
TRANSFER WHILE LESS, UPDATE	TLSU	(P)E8	3-131
TRANSFER WHILE NOT EQUAL, DESTRUCTIVE	TNED	(P)E5	3-131
TRANSFER WHILE NOT EQUAL, UPDATE	TNEU	(P)ED	3-131
TRANSFER WHILE TRUE, DESTRUCTIVE	TWTD	(V)D3	3-131
TRANSFER WHILE TRUE, UPDATE	TWTU	(V)DB	3-132
TRANSFER WORDS OVERWRITE DESTRUCTIVE	TWOD	(P)D4	3-129
TRANSFER WORDS OVERWRITE UPDATE	TWOU	(P)DC	3-129
TRANSFER WORDS, DESTRUCTIVE	TWSD	(P)D3	3-128
TRANSFER WORDS, UPDATE TRANSLATE	TWSU	(P)DB	3-129
TRANSLATE	TRNS	(V)D7	3-157
UNPACK ABSOLUTE, DESTRUCTIVE	UABD	(V)D1	3-154
UNPACK ABSOLUTE, UPDATE	UABU	(V)D9	3-155
UNPACK SIGNED, DESTRUCTIVE	USND	(V)D0	3-155
UNPACK SIGNED, UPDATE	USNU	(V)D8	3-155
VALUE CALL	VALC	(P)00 → 3F	3-133
VECTOR BRANCH	VEBR	(Z)EE	3-167
VECTOR EXIT	VXIT	(Z)E6	3-167
VECTOR FETCH	FTCH	(Z)00 → 3F	3-170
VECTOR STORE	STOR	(Z)40 → 7F	3-170

APPENDIX J
PROCESSOR OPERATORS, BY HEXADECIMAL CODE

MODE ID & HEX CODE	OPERATOR NAME	MNEMONIC	PAGE
(P)00 → 3F	VALUE CALL	VALC	3-133
(Z)00 → 3F	VECTOR FETCH	FETCH	3-170
(P)40 → 7F	NAME CALL	NAMC	3-133
(Z)40 → 7F	VECTOR STORE	STOR	3-170
(V)42	SET TWO SINGLES TO DOUBLE	JOIN	3-142
(V)43	SET DOUBLE TO TWO SINGLES	SPLT	3-142
(V)44	IDLE UNTIL INTERRUPT	IDLE	3-152
(V)45	SET INTERVAL TIMER	SINT	3-151
(V)46	ENABLE EXTERNAL INTERRUPTS	EEXI	3-151
(V)47	DISABLE EXTERNAL INTERRUPTS	DEXI	3-152
(V)48	IGNORE PARITY	IGPR	3-158
(V)4A	SCAN IN	SCNI	3-148
(V)4E	READ PROCESSOR IDENTIFICATION	WHOI	3-151
(P)80	ADD	ADD	3-105
(P)81	SUBTRACT	SUBT	3-106
(P)82	MULTIPLY	MULT	3-106
(P)83	DIVIDE	DIVD	3-106
(P)84	INTEGER DIVIDE	IDIV	3-106
(V)84	PAUSE UNTIL INTERRUPT	PAUS	3-158
(P)85	REMAINDER DIVIDE	RDIV	3-106
(V)85	OCCURS INDEX	OCRX	3-157
(P)86	INTEGERIZE, TRUNCATED	NTIA	3-106
(P)87	INTEGERIZE, ROUNDED	NTGR	3-106
(V)87	INTEGERIZE, ROUNDED, DOUBLE PRECISION	NTGD	3-107
(P)88	LESS THAN	LESS	3-123
(P)89	GREATER THAN OR EQUAL	GREQ	3-122
(P)8A	GREATER THAN	GRTR	3-122
(P)8B	LESS THAN OR EQUAL	LSEQ	3-122
(V)8B	LEADING ONE TEST	LOG2	3-107
(P)8C	EQUAL	EQUL	3-122
(P)8D	NOT EQUAL	NEQL	3-123
(P)8E	CHANGE SIGN BIT	CHSN	3-107
(P)8F	EXTENDED MULTIPLE	MULX	3-106
(V)8F	INTERRUPT CHANNEL N	INCN	3-159
(P)90	LOGICAL AND	LAND	3-120
(P)91	LOGICAL OR	LOR	3-121
(P)92	LOGICAL NEGATE	LNOT	3-121
(P)93	LOGICAL EQUIVALENCE	LEQV	3-121

PROCESSOR OPERATORS, BY HEXADECIMAL CODE

MODE ID & HEX CODE	OPERATOR NAME	MNEMONIC	PAGE
(P)94	LOGICAL EQUAL	SAME	3-123
(P)95	ESCAPE TO 16-BIT INSTRUCTION	VARI	3-143
(P)96	BIT SET	BSET	3-107
(P)97	DYNAMIC BIT SET	DBST	3-107
(P)98	FIELD TRANSFER	FLTR	3-139
(P)99	DYNAMIC FIELD TRANSFER	DFTR	3-139
(P)9A	FIELD ISOLATE	ISOL	3-139
(P)9B	DYNAMIC FIELD ISOLATE	DISO	3-142
(P)9C	FIELD INSERT	INSR	3-142
(P)9D	DYNAMIC FIELD INSERT	DINS	3-142
(P)9E	BIT RESET	BRST	3-107
(P)9F	DYNAMIC BIT RESET	DBRS	3-107
(P)A0	BRANCH FALSE	BRFL	3-108
(P)A1	BRANCH TRUE	BRTR	3-108
(P)A2	BRANCH UNCONDITIONAL	BRUN	3-108
(P)A3	EXIT	EXIT	3-136
(P)A4	STEP AND BRANCH	STBR	3-109
(P)A5	INDEX AND LOAD NAME	NXLN	3-118
(P)A6	INDEX	INDX	3-117
(P)A7	RETURN	RETN	3-139
(P)A8	DYNAMIC BRANCH FALSE	DBFL	3-109
(V)A8	SET MEMORY INHIBITS	SINH	3-158
(P)A9	DYNAMIC BRANCH TRUE	DBTR	3-108
(P)AA	DYNAMIC BRANCH UNCONDITIONAL	DBUN	3-108
(V)AA	SET MEMORY LIMITS	SLMT	3-158
(P)AB	ENTER	ENTR	3-136
(P)AC	EVALUATE DESCRIPTOR	EVAL	3-136
(V)AC	FETCH MEMORY FAIL	FMFR	3-158
(P)AD	INDEX AND LOAD VALUE	NXLV	3-118
(P)AE	MARK STACK	MKST	3-132
(P)AF	STUFF ENVIRONMENT	STFF	3-143
(V)AF	MOVE TO STACK	MVST	3-156
(P)B0	LIT CALL ZERO	ZERO	3-119
(P)B1	LIT CALL ONE	ONE	3-120
(P)B2	LIT CALL 8 BITS	LT8	3-120
(P)B3	LIT CALL 16 BITS	LT16	3-120

PROCESSOR OPERATORS, BY HEXADECIMAL CODE

MODE ID & HEX CODE	OPERATOR NAME	MNEMONIC	PAGE
(P)B4	PUSH DOWN STACK REGISTERS	PUSH	3-125
(V)B4	SET TAG FIELD	STAG	3-151
(P)B5	DELETE TOP OF STACK	DLET	3-125
(V)B5	READ TAG FIELD	RTAG	3-151
(P)B6	EXCHANGE	EXCH	3-125
(V)B6	ROTATE STACK UP	RSUP	3-125
(P)B7	DUPLICATE TOP OF STACK	DUPL	3-125
(V)B7	ROTATE STACK DOWN	RSDN	3-125
(P)B8	STORE DESTRUCTIVE	STOD	3-125
(V)B8	READ PROCESSOR REGISTER	RPRR	3-152
(P)B9	STORE NON-DESTRUCTIVE	STON	3-126
(V)B9	SET PROCESSOR REGISTER	SPRR	3-152
(P)BA	OVERWRITE DESTRUCTIVE	OVRD	3-126
(V)BA	READ WITH LOCK	RDLK	3-126
(P)BB	OVERWRITE NON-DESTRUCTIVE	OVRN	3-126
(V)BB	COUNT BINARY ONES	CBON	3-107
(V)BC	LOAD TRANSPARENT	LODT	3-118
(P)BD	LOAD	LOAD	3-118
(V)BD	LINKED LIST LOOKUP	LLLU	3-155
(P)BE	LIT CALL 48 BITS	LT48	3-120
(V)BE	MASKED SEARCH FOR EQUAL	SRCH	3-156
(P)BF	MAKE PROGRAM CONTROL WORD	MPCW	3-120
(V)BF	STOP	STOP	3-159
(P)C0	SCALE LEFT	SCLF	3-123
(P)C1	DYNAMIC SCALE LEFT	DSLF	3-123
(P)C2	SCALE RIGHT TRUNCATE	SCRT	3-124
(P)C3	DYNAMIC SCALE RIGHT TRUNCATE	DSRT	3-124
(P)C4	SCALE RIGHT SAVE	SCRS	3-124
(P)C5	DYNAMIC SCALE RIGHT SAVE	DSRS	3-124
(P)C6	SCALE RIGHT FINAL	SCRF	3-124
(P)C7	DYNAMIC SCALE RIGHT FINAL	DSRF	3-124
(P)C8	SCALE RIGHT ROUND	SCRR	3-124
(P)C9	DYNAMIC SCALE RIGHT ROUND	DSRR	3-124
(P)CA	INPUT CONVERT, DESTRUCTIVE	ICVD	3-119
(P)CB	INPUT CONVERT, UPDATE	ICVU	3-119
(P)CC	SET TO SINGLE PRECISION, TRUNCATED	SNGT	3-142

PROCESSOR OPERATORS, BY HEXADECIMAL CODE

MODE ID & HEX CODE	OPERATOR NAME	MNEMONIC	PAGE
(P)CD	SET TO SINGLE PRECISION, ROUNDED	SNGL	3-142
(P)CE	SET TO DOUBLE PRECISION	XTND	3-142
(P)CF	INSERT MARK STACK	IMKS	3-133
(E)D0	MOVE WITH INSERT	MINS	3-162
(P)D0	TABLE ENTER EDIT, DESTRUCTIVE	TEED	3-111
(V)D0	UNPACK SIGNED, DESTRUCTIVE	USND	3-155
(E)D1	MOVE WITH FLOAT	MFLT	3-162
(P)D1	PACK DESTRUCTIVE	PACD	3-121
(V)D1	UNPACK ABSOLUTE, DESTRUCTIVE	UABD	3-154
(E)D2	SKIP FORWARD SOURCE CHARACTERS	SFSC	3-163
(P)D2	EXECUTE SINGLE MICRO, DESTRUCTIVE	EXSD	3-112
(V)D2	TRANSFER WHILE FALSE, DESTRUCTIVE	TWFD	3-132
(E)D3	SKIP REVERSE SOURCE CHARACTERS	SRSC	3-163
(P)D3	TRANSFER WORDS, DESTRUCTIVE	TWSD	3-128
(V)D3	TRANSFER WHILE TRUE, DESTRUCTIVE	TWTD	3-131
(E)D4	RESET FLOAT	RSTF	3-163
(P)D4	TRANSFER WORDS, OVERWRITE DESTRUCTIVE	TWOD	3-129
(V)D4	SCAN WHILE FALSE, DESTRUCTIVE	SWFD	3-151
(E)D5	END FLOAT	ENDF	3-163
(P)D5	STRING ISOLATE	SIS0	3-128
(V)D5	SCAN WHILE TRUE, DESTRUCTIVE	SWTD	3-150
(E)D6	MOVE NUMERIC UNCONDITIONAL	MVNU	3-163
(P)D6	SET EXTERNAL SIGN	SXSN	3-143
(E)D7	MOVE CHARACTERS	MCHR	3-162
(P)D7	READ AND CLEAR OVERFLOW FLIP-FLOP	ROFF	3-143
(V)D7	TRANSLATE	TRNS	3-157
(E)D8	INSERT OVERPUNCH	INOP	3-161
(P)D8	TABLE ENTER EDIT, UPDATE	TEEU	3-112
(V)D8	UNPACK SIGNED UPDATE	USNU	3-155
(E)D9	INSERT DISPLAY SIGN	INSG	3-161
(P)D9	PACK UPDATE	PACU	3-122
(V)D9	UNPACK ABSOLUTE, UPDATE	UABU	3-155
(E)DA	SKIP FORWARD DESTINATION CHARACTERS	SFDC	3-163
(P)DA	EXECUTE SINGLE MICRO, UPDATE	EXSU	3-112
(V)DA	TRANSFER WHILE FALSE, UPDATE	TWFU	3-132

PROCESSOR OPERATORS, BY HEXADECIMAL CODE

MODE ID & HEX CODE	OPERATOR NAME	MNEMONIC	PAGE
(E)DB	SKIP REVERSE DESTINATION CHARACTERS	SRDC	3-163
(P)DB	TRANSFER WORDS, UPDATE	TWSU	3-129
(V)DB	TRANSFER WHILE TRUE, UPDATE	TWTU	3-132
(E)DC	INSERT UNCONDITIONAL	INSU	3-161
(P)DC	TRANSFER WORDS OVERWRITE UPDATE	TWOU	3-129
(V)DC	SCAN WHILE FALSE, UPDATE	SWFU	3-151
(E)DD	INSERT CONDITIONAL	INSC	3-161
(P)DD	EXECUTE SINGLE MICRO, SINGLE POINTER UPDATE	EXPU	3-112
(V)DD	SCAN WHILE TRUE, UPDATE	SWTU	3-151
(E)DE	END EDIT	ENDE	3-164
(P)DE	READ TRUE/FALSE FLIP-FLOP	RTFF	3-143
(E)DF	CONDITIONAL HALT	HALT	3-164
(P)DF	CONDITIONAL HALT	HALT	3-143
(V)DF	CONDITIONAL HALT	HALT	3-159
(P)E0	TRANSFER WHILE LESS, DESTRUCTIVE	TLSD	3-131
(Z)E0	LOAD A	LDA	3-167
(P)E1	TRANSFER WHILE GREATER OR EQUAL, DESTRUCTIVE	TGED	3-130
(Z)E1	LOAD A INCREMENT	LDAI	3-168
(P)E2	TRANSFER WHILE GREATER, DESTRUCTIVE	TGTD	3-129
(Z)E2	LOAD B	LDB	3-167
(P)E3	TRANSFER WHILE LESS OR EQUAL, DESTRUCTIVE	TLED	3-130
(Z)E3	LOAD B INCREMENT	LDBI	3-168
(P)E4	TRANSFER WHILE EQUAL, DESTRUCTIVE	TEQD	3-130
(Z)E4	LOAD C	LDC	3-167
(P)E5	TRANSFER WHILE NOT EQUAL, DESTRUCTIVE	TNED	3-131
(Z)E5	LOAD C INCREMENT	LDCI	3-168
(P)E6	TRANSFER UNCONDITIONAL, DESTRUCTIVE	TUND	3-132
(Z)E6	VECTOR EXIT	VXIT	3-167
(P)E7	SINGLE-WORD VECTOR MODE	VMOS	3-117
(Z)E7	MULTIPLE PROGRAM WORD ENTRY	VMOS	3-117
(P)E8	TRANSFER WHILE LESS, UPDATE	TLSU	3-131
(Z)E8	STORE A	STA	3-168
(P)E9	TRANSFER WHILE GREATER OR EQUAL, UPDATE	TGEU	3-130
(Z)E9	STORE A INCREMENT	STAI	3-168
(P)EA	TRANSFER WHILE GREATER, UPDATE	TGTU	3-130
(Z)EA	STORE B	STB	3-168
(P)EB	TRANSFER WHILE LESS OR EQUAL, UPDATE	TLEU	3-130
(Z)EB	STORE B INCREMENT	STBI	3-168
(P)EC	TRANSFER WHILE EQUAL, UPDATE	TEQU	3-130
(Z)EC	STORE C	STC	3-168

PROCESSOR OPERATORS, BY HEXADECIMAL CODE

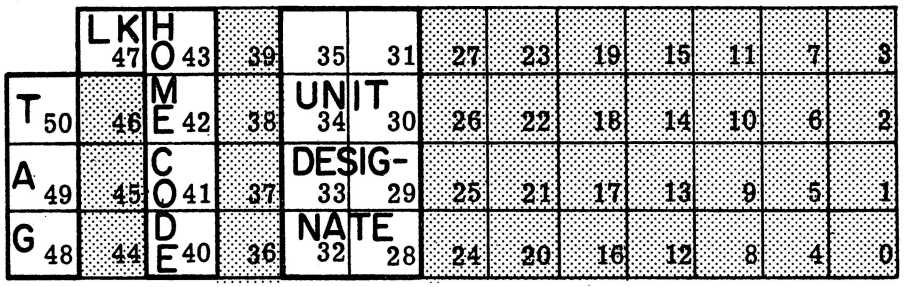
MODE ID & HEX CODE	OPERATOR NAME	MNEMONIC	PAGE
(P)ED	TRANSFER WHILE NOT EQUAL, UPDATE	TNEU	3-131
(Z)ED	STORE C INCREMENT	STCI	3-168
(P)EE	TRANSFER UNCONDITIONAL, UPDATE	TUNU	3-132
(Z)EE	VECTOR BRANCH	VEBR	3-167
(P)EF	MULTIPLE-WORD VECTOR MODE	VMOM	3-117
(Z)EF	MULTIPLE-WORD VECTOR MODE	VMOM	3-117
(P)F0	COMPARE CHARACTERS LESS, DESTRUCTIVE	CLSD	3-111
(V)F0	SCAN WHILE LESS, DESTRUCTIVE	SLSD	3-150
(Z)F0	DOUBLE LOAD A	DLA	3-168
(P)F1	COMPARE CHARACTERS GREATER OR EQUAL, DESTRUCTIVE	CGED	3-110
(V)F1	SCAN WHILE GREATER OR EQUAL, DESTRUCTIVE	SGED	3-149
(Z)F1	DOUBLE LOAD A INCREMENT	DLAI	3-169
(P)F2	COMPARE CHARACTERS GREATER, DESTRUCTIVE	CGTD	3-110
(V)F2	SCAN WHILE GREATER, DESTRUCTIVE	SGTD	3-148
(Z)F2	DOUBLE LOAD B	DLB	3-168
(P)F3	COMPARE CHARACTERS LESS OR EQUAL, DESTRUCTIVE	CLED	3-111
(V)F3	SCAN WHILE LESS OR EQUAL, DESTRUCTIVE	SLED	3-150
(Z)F3	DOUBLE LOAD B INCREMENT	DLBI	3-169
(P)F4	COMPARE CHARACTERS EQUAL, DESTRUCTIVE	CEQD	3-110
(V)F4	SCAN WHILE EQUAL, DESTRUCTIVE	SEQD	3-149
(Z)F4	DOUBLE LOAD C	DLC	3-168
(P)F5	COMPARE CHARACTERS NOT EQUAL, DESTRUCTIVE	CNED	3-111
(V)F5	SCAN WHILE NOT EQUAL, DESTRUCTIVE	SNED	3-150
(Z)F5	DOUBLE LOAD C INCREMENT	DLCI	3-169
(P)F8	COMPARE CHARACTERS LESS, UPDATE	CLSU	3-111
(V)F8	SCAN WHILE LESS, UPDATE	SLSU	3-150
(Z)F8	DOUBLE STORE A	DSA	3-169
(P)F9	COMPARE CHARACTERS GREATER OR EQUAL, UPDATE	CGEU	3-110
(V)F9	SCAN WHILE GREATER OR EQUAL, UPDATE	SGEU	3-149
(Z)F9	DOUBLE STORE A INCREMENT	DSAI	3-169
(P)FA	COMPARE CHARACTERS GREATER, UPDATE	CGTU	3-110
(V)FA	SCAN WHILE GREATER, UPDATE	SGTU	3-148
(Z)FA	DOUBLE STORE B	DSB	3-169
(P)FB	COMPARE CHARACTERS LESS OR EQUAL, UPDATE	CLEU	3-111
(V)FB	SCAN WHILE LESS OR EQUAL, UPDATE	SLEU	3-150

PROCESSOR OPERATORS, BY HEXADECIMAL CODE

MODE ID & HEX CODE	OPERATOR NAME	MNEMONIC	PAGE
(Z)FB	DOUBLE STORE B INCREMENT	DSBI	3-169
(P)FC	COMPARE CHARACTERS EQUAL, UPDATE	CEQU	3-110
(V)FC	SCAN WHILE EQUAL, UPDATE	SEQU	3-149
(Z)FC	DOUBLE STORE C	DSC	3-169
(P)FD	COMPARE CHARACTERS NOT EQUAL, UPDATE	CNEU	3-111
(V)FD	SCAN WHILE NOT EQUAL, UPDATE	SNEU	3-150
(Z)FD	DOUBLE STORE C INCREMENT	DSCI	3-169
(E)FE	NO OPERATION	NOOP	3-164
(P)FE	NO OPERATION	NOOP	3-143
(V)FE	NO OPERATION	NOOP	3-159
(Z)FE	NO OPERATION	NOOP	3-170
(E)FF	INVALID OPERATION	NVLD	3-164
(P)FF	INVALID OPERATION	NVLD	3-143
(V)FF	INVALID OPERATION	NVLD	3-159
(Z)FF	INVALID OPERATION	NVLD	3-170

APPENDIX K
IOM WORD FORMATS

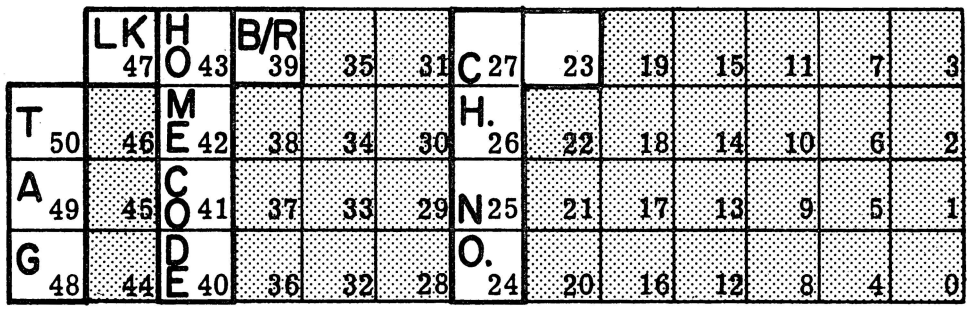
HA WORD 1, START I/O COMMAND



FIELD	BITS	DESCRIPTION
TAG	50:3	Denotes word is single precision (000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
-	46:3	Not used.
HOME CODE	43:4	Defines Start I/O command (0001).
-	39:4	Not used.
UNIT DESIGNATE	35:8	A unique 8-bit code-used with the UT base address to index and lock fetch from memory the UT word for the device to be started, and used with the QH base address to unlock fetch from memory the QH word, which points to the IOCB base address.
-	27:28	Not used.

41152

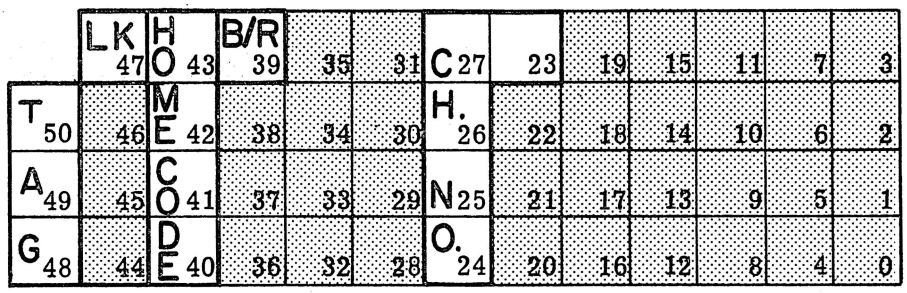
HA WORD 1, SET CHANNEL BUSY/RESERVED



FIELD	BITS	DESCRIPTION
TAG	50:3	Denotes word is single precision (000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
-	46:3	Not used.
HOME CODE	43:4	Defines Set CH Busy/Set CH Reserved Commands (0010).
B/R	39:1	When reset, further defines command as Set CH Busy; when set, further defines command as Set CH Reserved.
-	38:11	Not used.
CH. NO.	27:5	Identifies one of the 28 possible IOM channels.
-	22:23	Not used.

41153

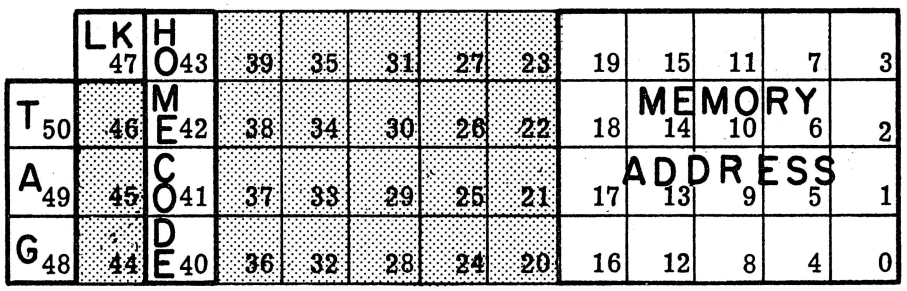
HA WORD 1, RESET CHANNEL BUSY/RESERVED



Field	Bits	Description
TAG	50:3	Denotes word is single precision (000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
--	46:3	Not used.
HOME CODE	43:4	Defines Reset CH Busy/Reset CH Reserved Commands (0011).
B/R	39:1	When reset, further defines command as Reset CH Busy; when set, further defines command as Reset CH Reserved.
--	38:11	Not used.
CH. NO.	27:5	Identifies one of the 28 possible IOM channels.
--	22:23	Not used.

41154

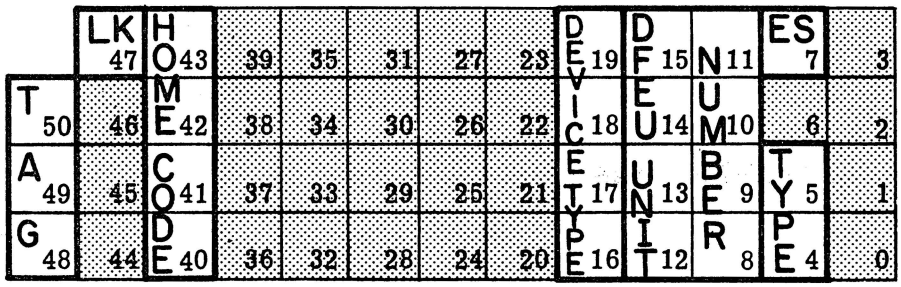
HA WORD 1, LOAD BASE ADDRESS (HA, UT, UOQH, SQ) COMMANDS



Field	Bits	Description
TAG	50:3	Denotes word is single precision (000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
--	46:3	Not used.
HOME CODE	43:4	Defines: (1) Load Home Address Command (0100) (2) Load Unit Table Address Command (0101) (3) Load I/O Queue Head Address Command (0110) (4) Load Status Queue Address (0111).
--	39:20	Not used.
MEMORY ADDRESS	19:20	The memory address to be stored in the Translator of the IOM to enable access of the IOM Job Map.

41155

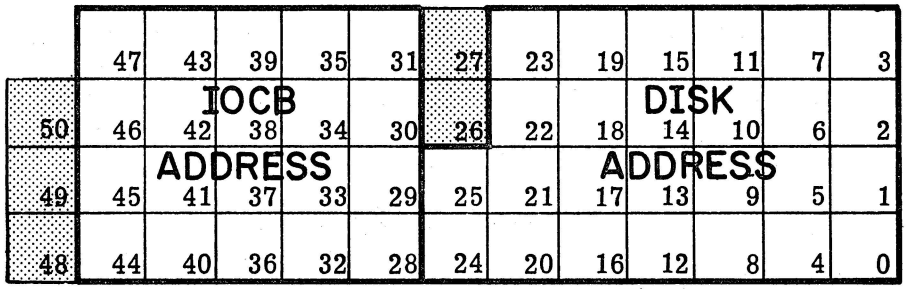
HA WORD 1, DFO SCAN-OUT COMMANDS (CLEAR STACK AND STORE CW REOUEST)



Field	Bits	Description
TAG	50:3	Denotes the word is single precision(000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
--	46:3	Not used.
HOME CODE	43:4	Defines the command as Scan Out (DFO or DCP) when 1000.
--	39:20	Not used.
DEVICE TYPE	19:4	Defines the Scan Out command is for a DFO (1001).
DFEU UNIT NUMBER and ES (EXCHANGE SELECT)	15:8 7:1	Together define the DFO by specifying a DFEU unit number and whether it is directly (bit 7=0) or indirectly (bit 7=1) connected to the DFO.
--	6:1	Not used.
TYPE	5:2	Defines the DFO Scan-Out command as Clear the Stack (10) or Store Control Word Request (01).
--	3:4	Not used.

41156

HA WORD 2, DFO SCAN OUT/STORE CONTROL WORD REQUEST COMMAND



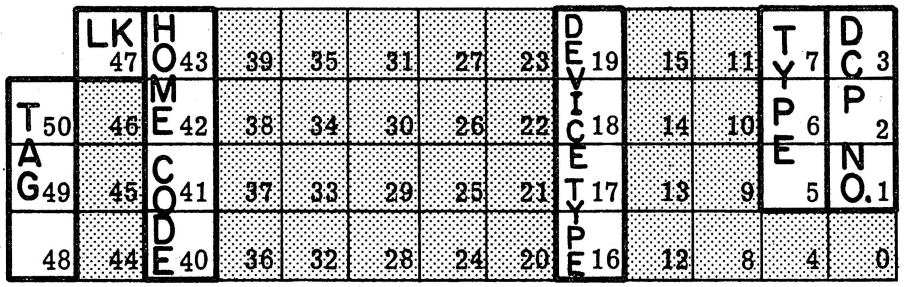
Field	Bits	Description
--	50:3	Not used.
IOCB ADDRESS	47:20	The base address of the job in memory.
--	27:2	Not used.
DISK ADDRESS	25:26	The disk address to be used for the job.

NOTE

This format also represents the format of the Scan Information word sent to the DFO.

41157

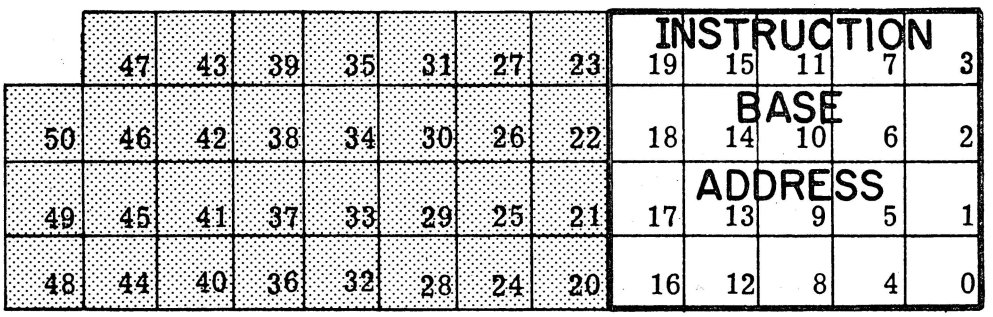
HA WORD 1, DCP SCAN-OUT COMMANDS (INITIATE, HALT, SET ATTENTION)



Field	Bits	Description
TAG	50:3	Denotes the word is single precision (000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
--	46:3	Not used.
HOME CODE	43:4	Defines the command as Scan Out (DFO or DCP) when 1000.
--	39:20	Not used.
DEVICE TYPE	19:4	Defines the Scan Out command is for a DCP (1100).
--	15:8	Not used.
TYPE	7:3	Defines the DCP Scan-Out command as Initiate (000), Halt (010), or Set Attention (100).
--	4:1	Not used.
DCP NO.	3:3	Defines the DCP for which the command is intended.
--	0:1	Not used.

41158

HA WORD 2, DCP SCAN-OUT/INITIATE COMMAND



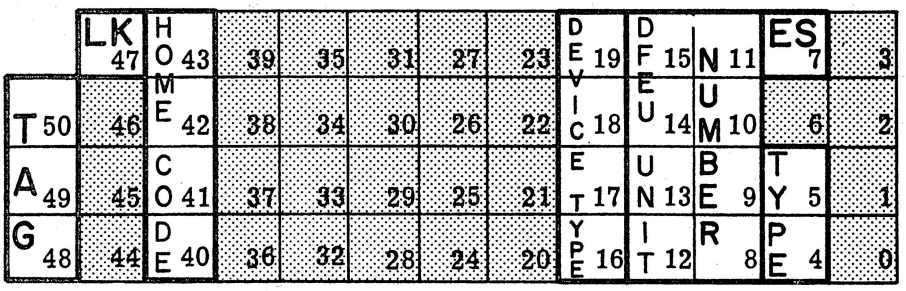
Field	Bits	Description
--	50:31	Not used.
INSTRUCTION BASE ADDRESS	19:20	Define the memory base address for the DCP code.

NOTE

This format also represents the format of the Scan Information word sent to the DCP.

41159

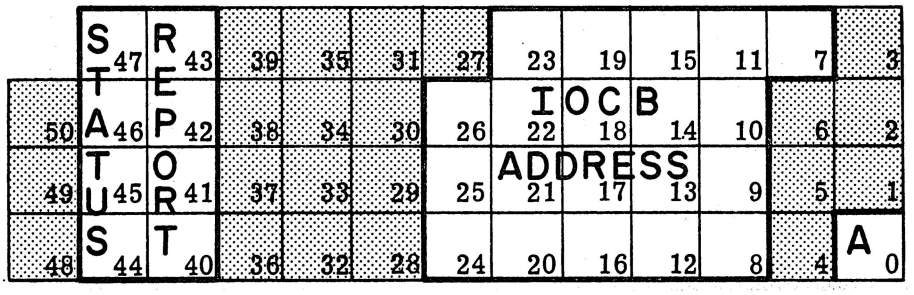
HA WORD 1, DFO SCAN-IN COMMANDS (QUEUED CONTROL WORD, TOP OF STACK, REPORT)



Field	Bits	Description
TAG	50:3	Denotes the word is single precision (000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
--	46:3	Not used.
HOME CODE	43:4	Defines the command as Scan In (1001).
--	39:20	Not used.
DEVICE TYPE	19:4	Defines the command as for a DFO (1001).
DFEU UNIT NUMBER and ES (EXCHANGE SELECT)	15:8 7:1	Together define the DFO by specifying a DFEU unit number and whether it is directly or indirectly connected to the DFO (via an exchange). These fields are not used for the Scan-In DFO Report Command.
--	6:1	Not used.
TYPE	5:2	Defines the DFO Scan-Out command as either Queued Control Word (01), Top of Stack (10), or Report (11).
--	3:4	Not used.

41160

HA WORD 2 (SCAN-IN WORD), SCAN-IN DFO QUEUED CONTROL WORD AND TOP OF STACK COMMANDS



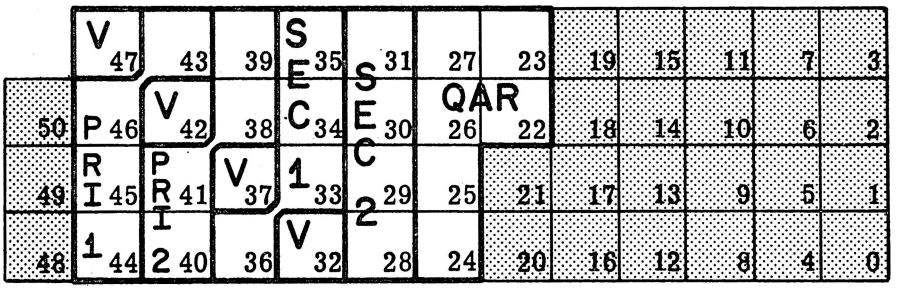
FIELD	BITS	DESCRIPTION
--	50:3	Not used.
STATUS REPORT	47:8	Describes the nature of the DFO by bits set as follows: (1) 47 set = No Access to Exchange (2) 46 set = SU Not Available (3) 45 set = Parity Error (4) 44 set = Disk Address Error (5) 43 set = Queded Control Word (6) 42 set = Top of Stack Control Word (7) 41 set = Stack Empty (8) 40 set = Control Word Not Available
--	39:13	Not used.
IOCB ADDRESS	26:20	Defines the memory address of the IOCB.
--	6:6	Not used.
A (ATTENTION)	0:1	When set, alerts the IOM to examine the STATUS REPORT FIELD.

NOTE:

This format also represents the format of the Scan Information word received from the DFO.

41161

HA WORD 2 SCAN-IN DFO REPORT COMMAND



FIELD	BITS	DESCRIPTION
-	50:3	Not used.
V	47:1	When true indicates connection of an EU/DFO bus at port 1 and the EUs connected to this bus are referenced by the EUD code present on lines 43-46 of the Scan Information Lines.
PRI 1	46:4	EUD code for port 1 bus (bit 46=MSB).
V	42:1	When true indicates connection of an EU/DFO bus at port 2 and the EUs connected to this bus are referenced by the EUD code present on lines 38-41.
PRI 2	41:4	EUD code for port 2 bus (bit 41=MSB).
V	37:1	When true indicates connection of an EU/DFO bus at port 3, and the EUs connected to this bus are referenced by the EUD code present on lines 33-36.
SEC 1	36:4	EUD code for port 3 bus (bit 36=MSB)
V	32:1	When true indicates connection of an EU/DFO bus at port 4, and the EUs connected to this bus are referenced by the EUD code present on lines 28-31.
SEC 2	31:4	EUD code for port 4 bus (bit 31=MSB).

NOTE

If a given EUD code appears on Scan Information lines 38-41 or 43-46, then the EUs referenced by the code are connected to the responding DFO in a direct manner, but if the EUD code appears on lines 28-31 or 33-36, then the EUs referenced by the EUD code are connected to the responding DFO indirectly (that is, via the other DFO of the DFO-pair).

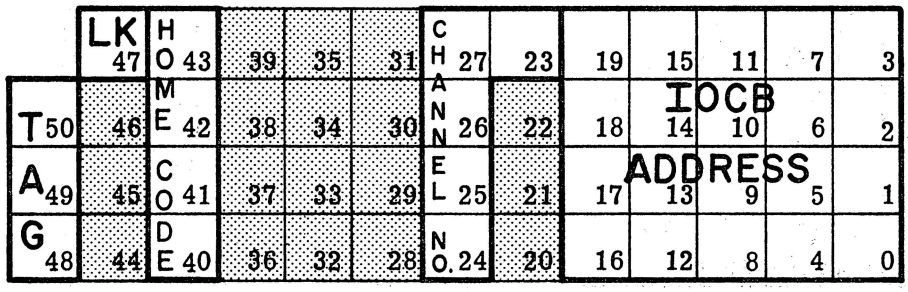
QAR	27:6	Indicates capacity of memory stack (bit 27=MSB).
-	21:22	Not used.

NOTE

This format also represents the format of the Scan Information word received from the DFO.

41162

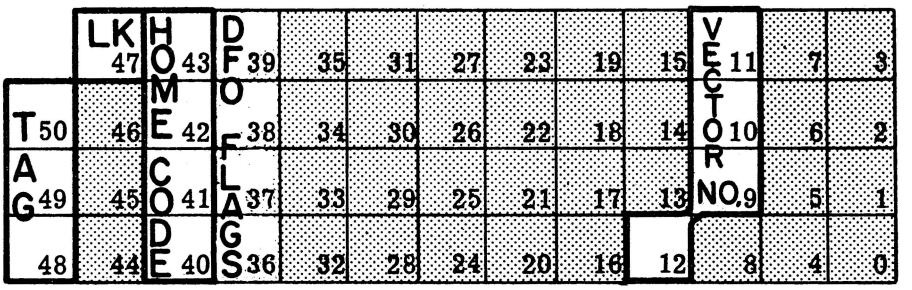
HA WORD 1, SYNC I/O COMMAND



Field	Bits	Description
TAG	50:3	Denotes the word is single precision(000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
--	46:3	Not used.
HOME CODE	43:4	Defines the command as Sync I/O.
--	39:12	Not used.
CHANNEL NO.	27:5	Identifies one of the 28 possible IOM channels.
--	22:3	Not used.
IOCB ADDRESS	19:20	The address of the job request in memory.

41163

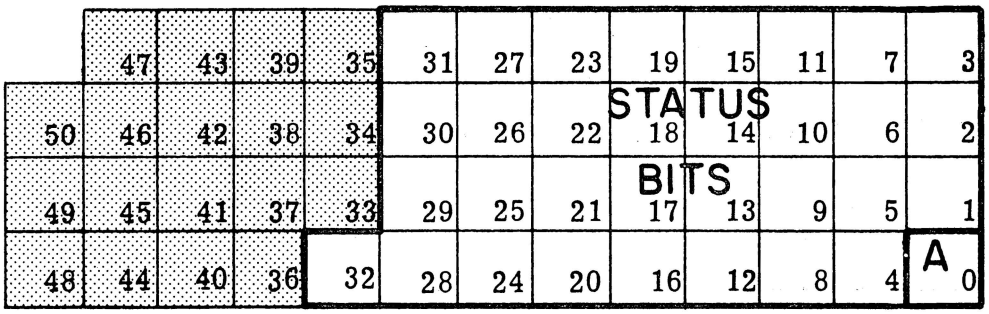
HA WORD 1, INTERROGATE PERIPHERAL STATUS COMMAND



Field	Bits	Description
TAG	50:3	Denotes the word is single precision(000).
LK	47:1	When set by software indicates the HA words are available for IOM use. Resets when IOM services HA words.
--	46:3	Not used.
HOME CODE	43:4	Defines Interrogate Peripheral Status Command (1011).
--	39:27	Not used.
VECTOR NO.	12:4	Defines the number of the status vector to be interrogated.
--	8:9	Not used.

41164

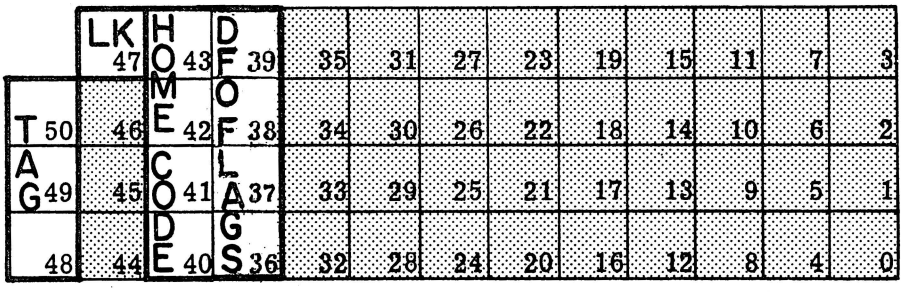
HA WORD 2 (STATUS WORD RETURNED), INTERROGATE PERIPHERAL STATUS COMMAND



Field	Bits	Description
--	50:18	Not used.
STATUS BITS	31:31	Each bit of this field, when on, indicates the ready status of the associated unit on the vector.
A	0:1	When set, alerts the IOM to examine the STATUS BITS field.

41165

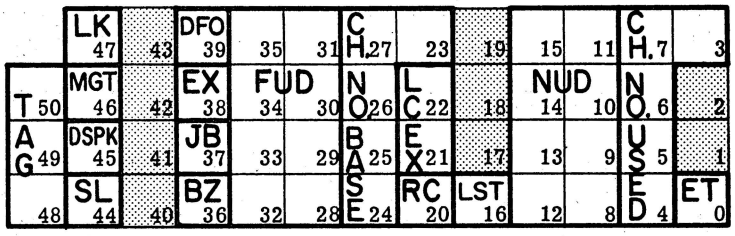
HA WORD 1, INHIBIT IOM, ACTIVATE IOM, AND LOAD DFO FLAGS COMMANDS



Field	Bits	Description
TAG	50:3	Denotes word is single precision(000).
LK	47:1	When set by software indicates the HA words are available for IOM services.
HOME CODE	43:4	Defines the command as follows: (1) 1100 = Inhibit IOM (2) 1101 = Activate IOM (3) 1110 = Load DFO Flags
	39:4	DFO Flags (for LOAD DFO FLAGS command only).
	35:36	Not Used.

41166

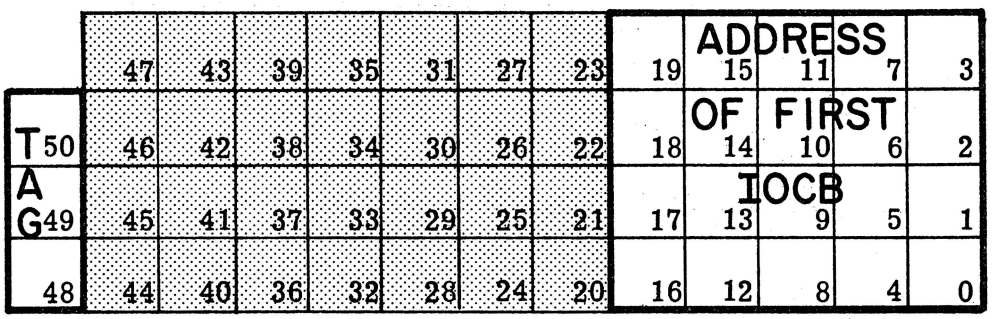
UNIT TABLE WORD



Field	Bits	Description
TAG	50:3	Denotes word is single precision(000).
LK	47:1	When set, indicates the UT word is being operated on.
MGT	46:1	When set, indicates this job request is for a magnetic tape. (Set by software.)
DSPK	45:1	When set, indicates this job request is for a disk pack. (Set by software.)
SL	44:1	When set, indicates the presence of a side link in IOCB+1.
--	43:4	Not used.
DFO	39:1	When set, indicates unit is under control of a DFO. A ring walk will not be performed with this bit set. (Set by software.)
EX	38:1	When set, indicates the unit is connected to an exchange. A ring walk will be performed (if the job bit is set) with this bit set. (Set by software.) Not used if bit 39 is set.
JB	37:1	When set, indicates that all channels associated with this request were busy, and when a channel becomes free and no further request are queued for that device, this job is to be done. (Set by IOM.) Used only with exch. devices (Bit 38=1). Not used with DFO (Bit 39).
BZ	36:1	When set, indicates that this unit is busy. (Set by IOM.)
FUD	35:8	Points to the First Unit Designate Number connected to the exchange.
CH. NO. BASE	27:5	For units not on an exchange, the number of the channel to which this unit is connected. For units on an exchange, the lowest numbered channel to which the exchange is connected. NOTE CN 0 and 21 through 23 are unassigned and will cause a fail.
LCEX	22:2	Indicates the 2 least significant bits of the last channel number of the exchange, for the device to be used.
RC	20:1	When set, permits this unit to use a reserved channel.
--	19:3	Not used.
LST	16:1	When set, indicates this is the last Unit Designate on the exchange.
NUD	15:8	Points to the Next Unit Designate number connected to the exchange.
CH. NO. USED	7:5	These bits specify the channel that was used to service the device. (Set by IOM.)
--	2:2	Not used.
ET	0:1	When set, indicates that an error condition has been reported in the current Result Descriptor, and therefore additional jobs should not be initiated for the unit. This bit is normally reset by software.

41167

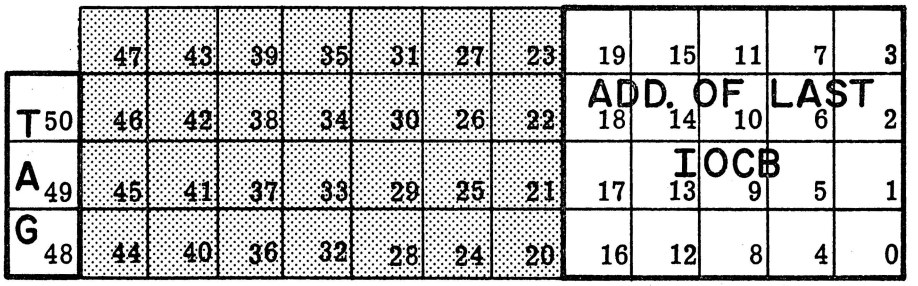
IOQH WORD



Field	Bits	Description
TAG	50:3	Denotes word is single precision (000).
--	47:28	Not used.
ADDRESS OF FIRST IOCB	19:20	Address of 1st IOCB in the IOQ. If bits 19-0 are null (zero), the UT word is unlocked and restored to memory.

41168

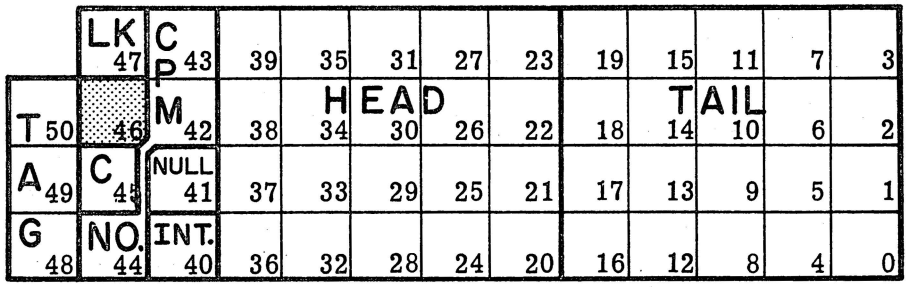
IOQT WORD



Field	Bits	Description
TAG	50:3	Denotes word is single precision (000).
--	47:28	Not used.
ADD OF LAST IOCB	19:20	Address of last IOCB in the IOQ.

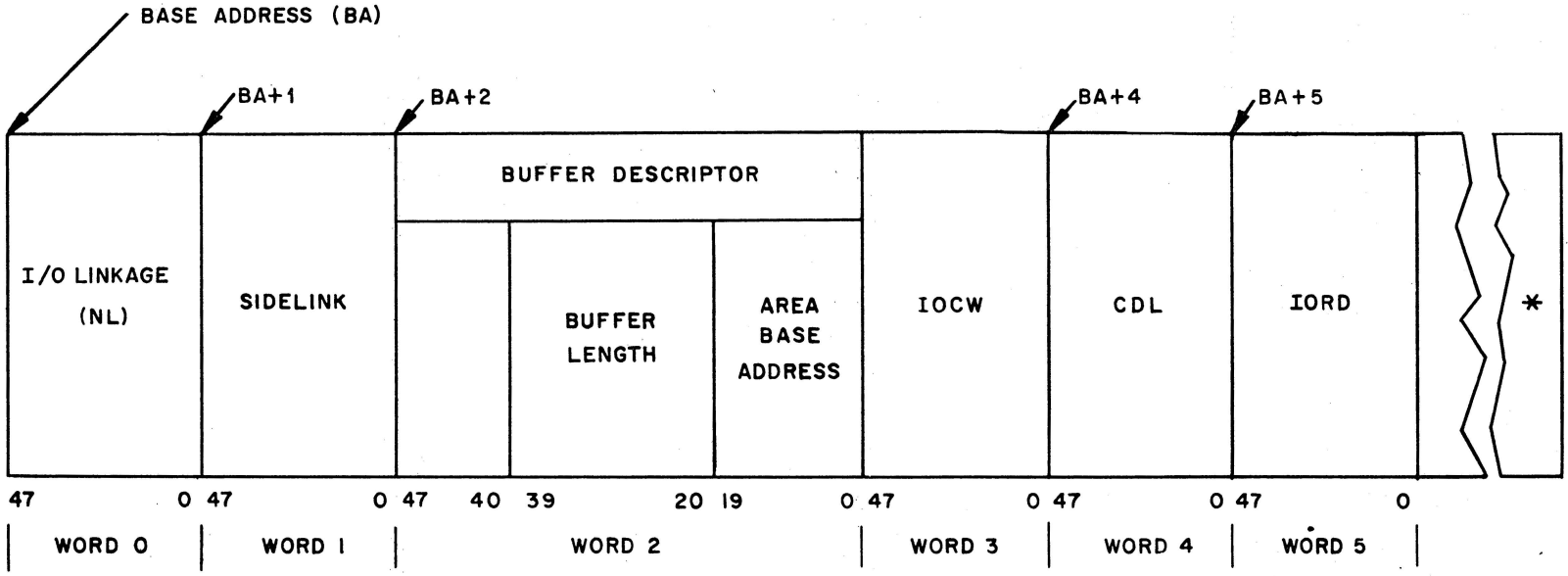
41169

SQH WORD



FIELD	BITS	DESCRIPTION
TAG	50:3	Denotes word is single precision (000).
LK	47:1	When set, indicates the SQH word is being operated on.
--	46:1	Not used.
C	45:1	Notifies software, when set, that a status change vector has occurred.
CPM NO.	44:3	Points to the CPM that will be interrupted by either channel interrupt or error interrupt.
NULL	41:1	When a 0, indicates that the queue is empty; when a 1, indicates terminated jobs are under queue.
INT	40:1	When set, (set by software) indicates that the CPM number field shall be interrupted upon job termination. (Reset by IOM)
HEAD	39:20	A 20-bit address pointing to the IOCB of the first device terminated. (Not used if bit 41 = 0)
TAIL	19:20	A 20-bit address pointing to the IOCB of the last device terminated. (Not used if 41 = 0)

41170

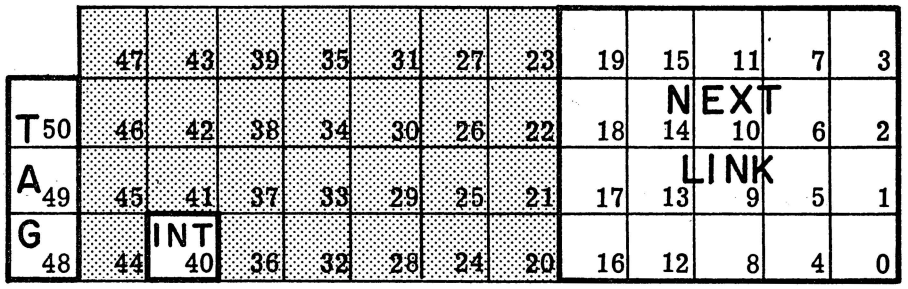


(IOCB)

* WORDS 6 THRU N ARE RESERVED FOR SOFTWARE USE ONLY

40177

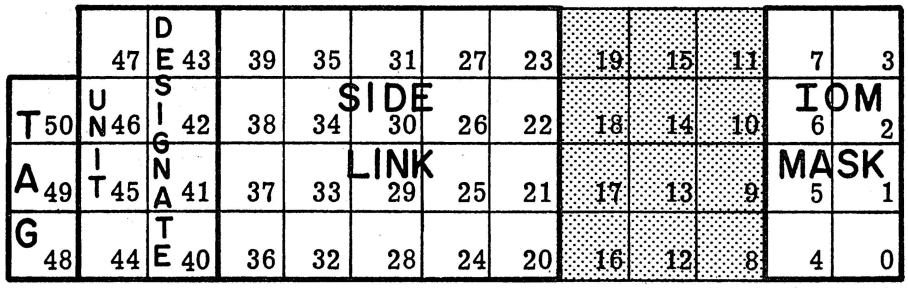
IOCB I/O LINKAGE (N/L) WORD (IOCB WORD 0)



FIELD	BITS	
TAG	50:3	Denotes word is single precision (000).
--	47:7	Not used.
INT	40:1	When set, notifies the IOM to interrupt the CPM specified in the SQ word upon completion of this job.
--	39:20	Not used.
NEXT LINK	19:20	Memory address of the next job (IOCB) queued for this device.

41171

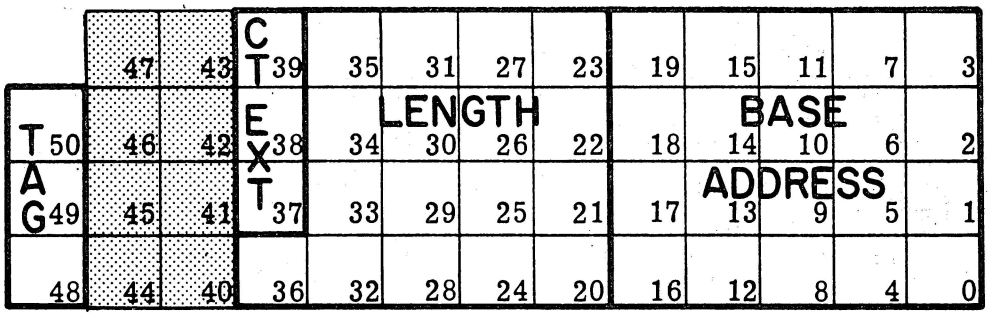
IOCB SIDELINK (SL) WORD (IOCB WORD 1)



FIELD	BITS	DESCRIPTION
TAG	50:3	Denotes the word is single precision(000).
UNIT DESIGNATE	47:8	Defines the device which is to perform this sidelinked job.
SIDE LINK	39:20	Memory address of the sidelinked job.
-	19:12	Not used.
IOM MASK	7:8	Defines an IOM channel number and thus defines the IOM (or IOM's) which can perform the sidelinked job.

41172

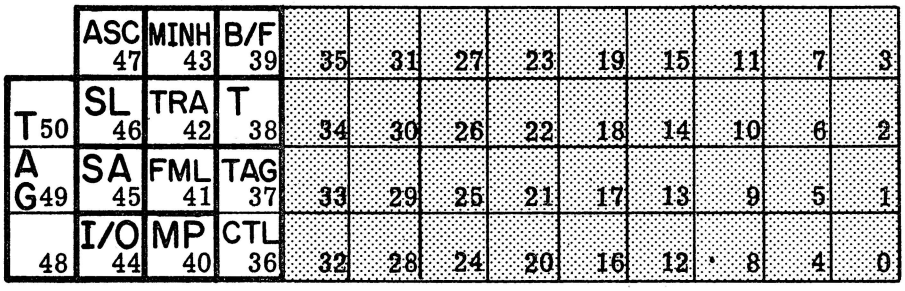
IOCB BUFFER DESCRIPTOR (BD) WORD (IOCB WORD 2)



FIELD	BITS	DESCRIPTION
TAG	50:3	Denotes word is single precision (000).
-	47:8	Not used.
CT EXT	39:3	If the length of the buffer includes a fractional part of a word, this field describes the number of characters in that fractional part.
LENGTH	36:17	Describes the length of the buffer in words. (Excess characters are described by the CT EXT field.)
BASE ADDRESS	19:20	Describes the memory address of the first data word of the buffer.

41173

IOCW (IOCB WORD 3)

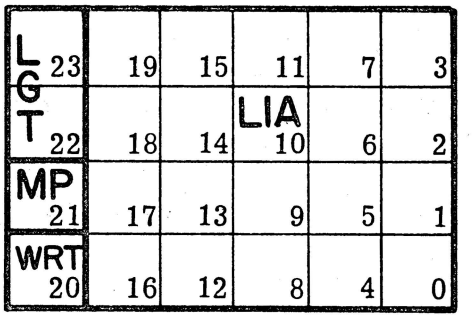


FIELD	BITS	DESCRIPTION
TAG	50:3	Denotes the word is single precision (000).
ASC	47:1	When set, indicates that ASCII translation is required.
SL	46:1	When set, indicates that a sidelink to another IOCW is required. (The address of the new IOCW is stored in bits 0 thru 19 of the IOCB SL word.)
SA	45:1	When set, will cause bit 1 of the result descriptor word (the Exception bit) to be set.
I/O	44:1	When set, indicates that the transfer is to be an input operation. When reset, indicates that the transfer is to be an output operation.
MINH	43:1	When set, indicates that data will not be transferred to/from memory.
TRA	42:1	When set, indicates that internal IOM translation is needed.
FML	41:1	When set, indicates that the frame length is to be 8-bits. When reset, indicates that the frame length is to be 6-bits.
MP	40:1	When set, indicates that a memory protect interrupt will occur if an attempt is made to store into a word in memory which has bit 48 = 1. The store will not occur.
B/F	39:1	When set, indicates a backward operation on a tape unit. When reset, indicates a forward operation on a tape unit.
T	38:1	When set, indicates a test operation.
TAG CTL	37:2	Indicates the following:
	35:36	Not used.

37	36	
0	0	Store single precision tags
1	1	Store double precision tags
0	1	Store program tags
1	0	Tag field transfer

41174

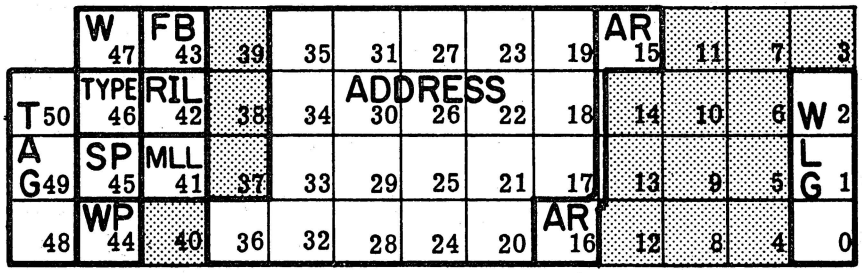
UNIT CONTROL WORD (UCW)



Field	Bits	Description
LGT	23:2	Specify the total length of the field being transferred as follows: 23 22 0 1 = Transfer 1 word 1 0 = Transfer 2 words
MP	21:1	On a one or two word store, if bit 48 of the information word already stored in that memory location is a one (protected word), memory shall not perform the store but shall send an error signal to the requestor.
WRT	20:1	Shall identify the service request as a Read (WRT=0) or Write (WRT=1) operation.
LIA	19:20	Shall specify the absolute starting memory address of the transfer.

41175

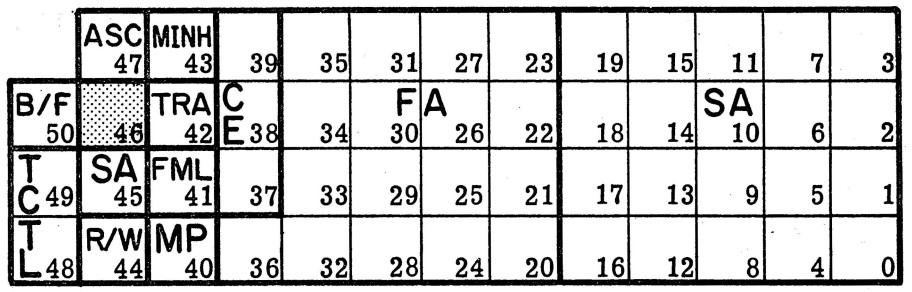
MEMORY CONTROL WORD



Field	Bits	Description
TAG	50:3	Not significant for control purposes; examined only for generation of parity.
W (Write)	47:1	When a 0 specifies that a read/restore operation is to be performed. When a 1, specifies that one of the write variations, as defined by the TYPE field, is to be performed.
TYPE	46:1	When the W field is a 1, specifies which write variation is to be performed as follows: when 46=0, a Clear/Write operation shall be performed (the Overwrite and Single-Word protected Write operations use this variation). When 46=1, a Read/Modify/Restore operation shall be performed (the N-Word Protected Write operation uses this variation). When the field is a 0 and 46=1, the contents of the Fail Register are fetched.
SP (Specifier)	45:1	When a 1, indicates that a single-word operation is to be performed. When a 0, indicates that an N-word operation is to be performed.
WP (Write Protect)	44:1	When a 1, indicates that a Protected Write operation is to be performed. It is a 0 if any other type of operation is specified.
FB (Flashback)	43:1	When a 1, specifies that the original contents of the memory location are to be sent to the requestor.
RIL (Requestor Inhibit Load)	42:1	Used in a Single-Word Overwrite operation to specify that a Load Requestor operation is to be performed. When a 1, specifies that the next data word sent to the MCM be loaded into the Requestor Inhibit Register instead of into memory.
MLL (Memory Limits Load)	41:1	When a 1, specifies that the next data word sent to the MCM be loaded into the Memory Limit Registers and the Available Register, instead of into memory.
ADDRESS	36:20	Specify the starting address for the memory operation.
AR (Address Residue)	16:2	Indicate the proper value (00, 01, or 10) that result from changes in the ADDRESS field.
--	14:12	Not used.
WLG (Word Length)	2:3	Indicates the number of words to be transferred during memory operations (2 words maximum).

41176

JOB WORD 1 (JW1) TO DSU



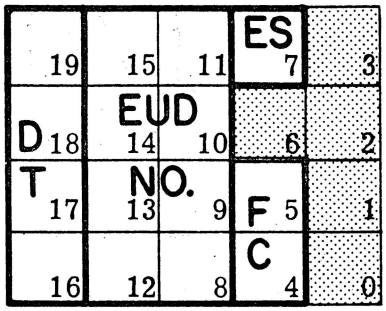
Field	Bit	Description
B/F (Backward/ Forward)	50:1	When set, indicates a backward/tape operation, and the address contained in the FA (final address) field should be used as the starting address.
T CTL (Tag controls)	49:2	Indicates source and type of tags for data words.
ASC	47:1	Indicates ASCII translation required.
--	46:1	Not used.
SA	45:1	When set, will cause bit 1 of the result descriptor word (the Exception bit) to be set.
R/W	44:1	When set, data is to be read from device; when reset, data is to be written to the device.
MINH	43:1	When set, no memory accesses are granted.
TRA	42:1	When set, code translation of data is required.
FML	41:1	When set, indicates that the frame length is 8 bits; when reset, indicates that the frame length is 6 bits.
MP	40:1	When set, indicates that a memory protect interrupt will occur if an attempt is made to store into a word in memory which has bit 48=1. The store will not occur.
CE	39:3	Number of characters in last data word.
FA	35:20	Final address, or last address in memory to be accessed (used as the first address to be accessed for backward-tape jobs).
SA	19:20	Starting address, or first address in memory to be accessed (used as the last address to be accessed for backward-tape jobs).

NOTE:

The format of the second job word sent to the DSU (JW2) is dependent upon the device, and is identical to the CDL word of the IOCB (IOCB word 4). For the formats of all possible CDL words, refer to Chapter IV, Section 3 of this manual.

41177

DFO SCAN ADDRESS WORD (SCAN-IN AND SCAN-OUT)

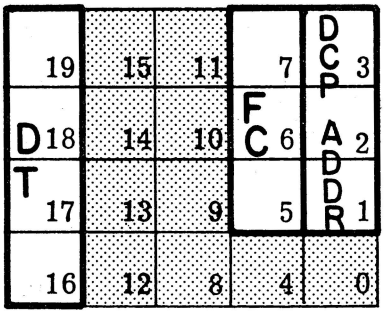


FIELD	BITS	DESCRIPTION
DT	19:4	Identifies the information as for a DFO (1001).
EUD NO. AND ES (EXCHANGE SELECT)	15:8 7:1	Together define the DFO by specifying a DFEU unit designate number and whether it is directly or indirectly connected to the DFO (via an exchange). These fields are not used if Scan-In DFO Report is the job to be implemented.
-	6:1	Not used.
FC	5:2	Function code which defines the operation as follows: (1) During Scan-Out: $\frac{5}{0}\ \frac{4}{1}$ = Store CW Request 1 0 = Clear-the-Stack (2) During Scan-In: $\frac{5}{0}\ \frac{4}{1}$ = Queued CW Request 1 0 = Top-of-Stack Request 1 1 = Report Request
-	3:4	Not used.

The format of the DFO Scan Address word may be related directly to bits 0 through 19 of HA word 1, when HA word 1 contains a command for DFO scan-out or scan-in.

41178

DCP SCAN ADDRESS WORD



FIELD	BITS	DESCRIPTION
DT	19:4	Defines the Scan-Out command is for a DCP (1100).
--	15:8	Not used.
FC	7:3	Defines the DCP Scan-Out command as Initiate (000), Halt (010), or Set Attention (100).
--	4:1	Not used.
DCP ADDR	3:3	Defines the DCP for which the command is intended.
--	0:1	Not used.

NOTE

The format of the DCP Scan Address word may be related directly to bits 0 through 19 of HA word 1, when HA word 1 contains a DCP scan-out command.

41179

BURROUGHS CORPORATION
DATA PROCESSING PUBLICATIONS
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DATE: 1-73

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